UNDERSTANDING AND DEVELOPMENT OF DIELECTRIC PASSIVATED HIGH EFFICIENCY SILICON SOLAR CELLS USING SPIN-ON SOLUTIONS

A Dissertation
Presented to
The Academic Faculty
by

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In Partial Fulfillment
of the Requirements for the Degree

Doctor of Philosophy in
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2012

UNDERSTANDING AND DEVELOPMENT OF DIELECTRIC PASSIVATED HIGH EFFICIENCY SILICON SOLAR CELLS USING SPIN-ON SOLUTIONS

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I dedicate this work to my late grandfather,
Mr.T.V.Muthuswamy.

ACKNOWLEDGEMENTS

I would like to begin by thanking my advisor Dr. Ajeet Rohatgi for his guidance, support and encouragement in ensuring the successful completion of this work. I have learnt a lot, both personally and professionally, under his tutelage. I would also like to thank members of my thesis committee, Dr. Kippelen, Dr.Begovic, Dr. Keezer and Dr.Melkote for their feedback and suggestions, which helped improve this work.

I would like to acknowledge all current and former members of UCEP, for their help with numerous experiments, technical discussions and friendship. Interactions with my colleagues have contributed to a fun and enriching experience at Georgia Tech and helped shape this research into its current form. I would also like to thank Adam Payne and Suniva for permitting the use of their facilities and tools for this research.

I would like to thank my wife for being not only my partner in life but also being an equal partner in my doctoral work. I would also like to thank my parents for their constant and unconditional support, patience and encouragement throughout the course of this doctoral work. Without their presence of my family by my side, this journey would've been impossible. I would also like to acknowledge all my friends, Arsenal F.C., Queen and Pink Floyd for providing me with the necessary distractions and entertainment to keep me sane.

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LIST OF SYMBOLS AND ABBREVIATIONS

PV	Photovoltaics
Si	Silicon
Ga	Gallium
B	Boron
P	Phosphorous
FZ	Float zone
Cz	Czhochralski
BSF	Back surface field
LBSF	Local Back surface field
SRV	Surface recombination velocity
BSRV	Back surface recombination velocity
FSRV	Front surface recombination velocity
BSR	Back surface reflectance
LBIC	Light beam induced current
IQE	Internal quantum efficiency
PECVD	Plasma enhanced chemical vapor deposition
SRH	Shockley-Reed-Hall
$\mathbf{V_{oc}}$	Open-circuit voltage
$\mathbf{J_{sc}}$	Short-circuit current density
FF	Fill factor
SEM	Scanning electron microscope
FGA	Forming gas anneal

UV	Ultra-violet
IR	Infra-red
LID	Light induced degradation
NREL	National renewable energy laboratory
PERC	Passivated emitter and rear cell
PERL	Passivated emitter, rear locally diffused
J_0	Reverse saturation current density
Å	Angstrom
µm	Micron
Ω	Ohm

SUMMARY

This thesis successfully demonstrated the use of spin-on solutions in the fabrication of high efficiency cells. A diffusion process was designed using in-house developed Phosphoric acid dopant solutions and optimized to produce emitters with high surface concentration and optimal emitter profile. Optimal gas-flow was identified as an important factor for uniform emitter formation. In addition, the process was modified to include a short pre-oxidation step after wafer loading that resulted in emitters with higher uniformity of diffusion and lower emitter saturation current density (< 100 fA/cm^2). This modified diffusion process was also more reproducible as it was insensitive to ambient humidity, unlike earlier processes using spin-on dopants. This emitter was first used to fabricate full Al BSF conventional cells (4 cm^2) with screen printed contacts, which led to cell efficiencies > 19.0%. This represents the highest efficiency for a screen printed full BSF cells. Further analysis and characterization showed that a high quality in-situ oxide passivation of the emitter along with very good screen printed contacts contributed to this high efficiency.

This high quality emitter was then used with a spin-on dielectric for the fabrication of a local BSF cell structure in which more than 95% of the rear surface was passivated by a dielectric with local contacts and back- surface field over the remaining area. Fabrication of such a device would generally require multiple high temperature steps. A simple streamlined process was designed that produced a diffused and passivated device in just a single high temperature step. Phosphoric acid based spin-on dopant sources were used for emitter diffusion and a spin-on dielectric was used for rear passivation. This process,

called Delta-STAR, resulted in diffusion of phosphorous only on the emitter side of the wafe. An in-situ oxidation step was also performed immediately after diffusion, which resulted in improved emitter passivation and anneal of the rear passivating dielectric. Peak efficiencies of ~20% were obtained on research size 4 cm^2 cells using this process in combination with screen printing for definition of rear vias and front and rear contacts. Nine 4 cm^2 cells were fabricated on 4 inch diameter, 300 μm thick FZ substrates. Characterization of these cells revealed that this improved efficiency for the local BSF cells resulted from an improvement in BSRV from 325 cm/s to 125 cm/s and in BSR from 67% to 93% compared to full BSF cells. These two factors contributed equally (~0.5) to the efficiency increase of 1% (absolute) for local BSF cells compared to their counterpart baseline cells.

A screen-printed etching process was used first to define the local vias through the dielectric but was found to be non-uniform, resulting in inconsistent solar cell performance. However, it did produce 20% efficient cells in the best case. This non-uniformities in the etching process resulted in formation of parasitic current paths between the rear contacts and inverted silicon underneath the rear dielectric. An alternate processing route was required to ensure improved reproducibility of this technology and insensitivity to substrate thickness, dielectric thickness and surface quality. Several laser candidates were investigated in this work for replacing the screen-printed method of via definition. High efficiency local BSF cells were fabricated using a UV laser for selective rear dielectric removal. The performance of the cells fabricated by UV laser ablation and screen-printed etching paste was very similar. Observation of the laser ablated vias under

an optical microscope and SEM indicated that the vias formed using lasers had some amount of surface damage, but compensated by the formation of a good uniform BSF. Further cell characterization and analysis indicated that the overall quality of the rear passivation was maintained, which was also supported by SEM analysis and PC1D modeling. Laser ablation was found to provide a fast and reproducible alternative to the screen printed etching process. Initial ablation of the dielectric using the UV laser was performed using 5 pulses to replicate the rear geometry of the screen-printed method. The rear geometry was then modified to use vias defined using a single pulse. The replacement of the 5 pulse process by the 1 pulse process resulted in higher throughput while improving the quality of the vias and reducing chances of parasitic shunts. The flexibility offered can help optimize the rear contact design further resulting in an increase in efficiency beyond 20.5 % and provide a more commercially viable alternative for fabrication of high efficiency thin cells. Alternate lasers were considered for rear ablation. Carbon dioxide lasers were able to produce high efficiency but suffered from wafer breakage due to too much melting and solidification of Si in the vias. A fiber laser with 1064 nm wavelength also resulted in high efficiency when optimized, but suffers from low throughput. In general, lasers operated in the continuous wave mode are deemed unsuitable for this purpose. Preliminary results in this study identify the green laser as a viable candidate that can be used for future studies without loss in cell performance or throughput.

To improve the manufacturability of these local BSF devices, they had to be fabricated on more inexpensive commercial substrates. Modeling was performed to understand the

impact of substrate thickness and bulk lifetime on local BSF cell efficiency. Since the development work involved polished FZ wafers, first the effect of surface finish on these devices was investigated. Surface roughness was tailored using KOH solution based treatments. Local BSF cells fabricated on double side textured wafers failed and it was found that reduced surface roughness was very critical for rear passivation and cell performance. KOH planarized rear surface with an RMS surface roughness of ~0.75 μm was found to be adequate and produced cell results comparable to those on polished FZ substrates. Using such surfaces cell efficiencies of ~20% on 180 μm mCz and ~19.4% on 150 μm Cz substrates were achieved. PC1D modeling was used to study the effect of substrate resistivity on LBSF cell efficiencies. Based on experimental data on surface passivation structures and device modeling, it was concluded that Cz substrate resistivities of 1-3 ohm.cm were optimum for local BSF solar cell performance after LID.

This research has developed technology and prototype cells to provide guidelines for fabrication of high efficiency solar cells using a local BSF design. When implemented optimally, the local BSF design can improve cell efficiency significantly (~1% absolute) over the conventional full Al BSF devices on thinner and inexpensive substrates. This cell design can provide a reduction in the $/W of solar energy and bring PV technology closer to grid parity.

CHAPTER 1

INTRODUCTION AND PROBLEM STATEMENT

1.1 Motivation

As we enter the 21st century, the demand for energy is expected to rise rapidly along with the awareness of environmental issues, pollution and the phenomenon of global warming. The reliance on conventional sources, like oil and coal, has come under increased scrutiny in the recent decades, because the increased usage of these sources has been linked to increased global mean temperatures, as seen in figure 1.1[1]. As the world looks to decrease its dependence on fossil fuels and attain energy independence simultaneously, sources that can provide a clean and economical alternative are being investigated. This has brought increased attention to renewable energy sources, though they still account for less than 10% of all energy consumed in the U.S, as seen in figure 1.2 [2]. Solar electricity or photovoltaics (PV) is one such alternative that has been gradually gaining momentum in the last decade, increasing at an average annual growth rate of 40%. The beauty of solar energy from the sun is that it is free, unlimited, clean and not localized in any part of the world. PV is a great way to convert sunlight into electricity, because it is safe, and it produces energy when it is most needed and is most expensive. It has been surmised that a large strategically-located solar farm of area 100×100 miles can help generate the energy that is consumed annually in the entire continental US.

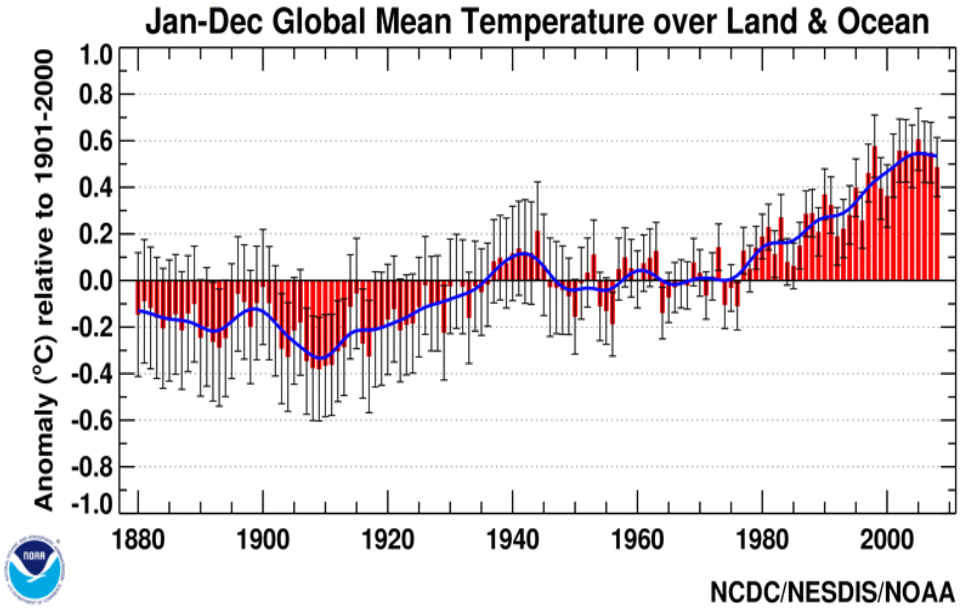


Figure 1.1: Increase in global mean temperature over the last 130 years

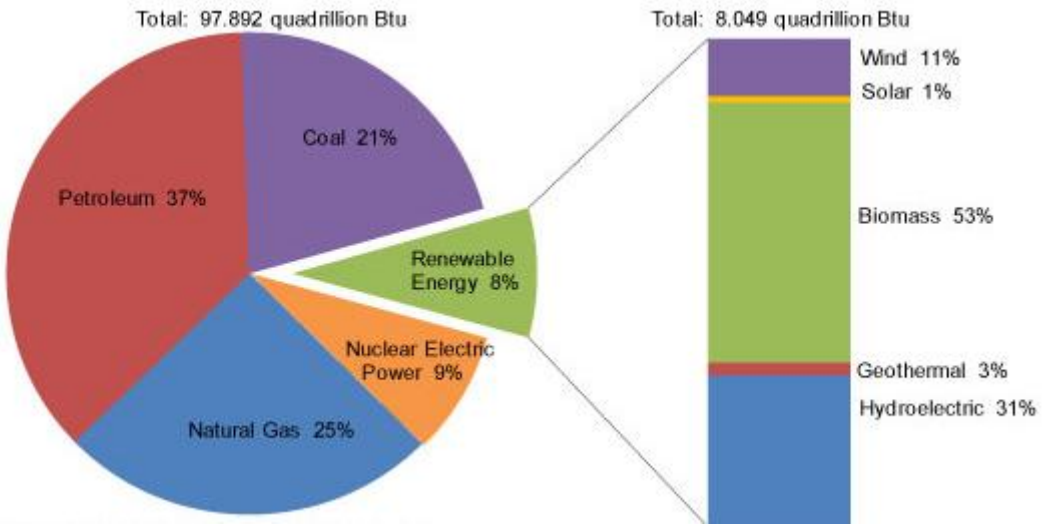


Figure 1.2: Contribution of various sources of energy to total U.S consumption in 2010 [2]

1.2 Challenges facing the growth of PV industry

The only challenge in PV is to reduce the cost, which is currently about a factor of 1.5-2 higher than conventional fossil fuels. The learning curve for PV shows that every time you double the amount of installed PV power in the world, the cost drops by ~20%. The

ultimate goal is to achieve an end-user cost of PV power that is comparable to that obtained from conventional sources, otherwise known as grid parity. The PV industry has consistently increased their share in the energy sector and, as an industry has shown a growth rate of ~40% over the last few years. Therefore, PV is expected to achieve grid parity within this decade, without the assistance of subsidies. Si is the dominant PV material today, which accounts for ~90% of all the PV modules shipped today. Crystalline Si PV module prices have dropped by almost 40% in 2011 and are approaching \$1/ W_p. However the right combination for price and efficiency is still not there for grid parity. Several routes have been identified to reduce the cost (\$/W) of solar power. In recent years, there has been increased competition from thin film PV technologies, especially CdTe, which have increased their market share to over 30% in the U.S. Crystalline silicon has been the longstanding leader in the field and has consistently maintained a market share over 60% in the U.S and over 85% worldwide. However, there are changes all over the crystalline Si landscape too. These changes range from feedstock preparation, crystal growth and ingot slicing at the materials end, to low-cost manufacturable technology development to increase cell efficiencies and lower the manufacturing cost at the cell and module level. Some of these efforts are beginning to have an effect as Si PV has recently rallied against the increased demand for thin film solar cells as seen in Figure 1.3 [2].

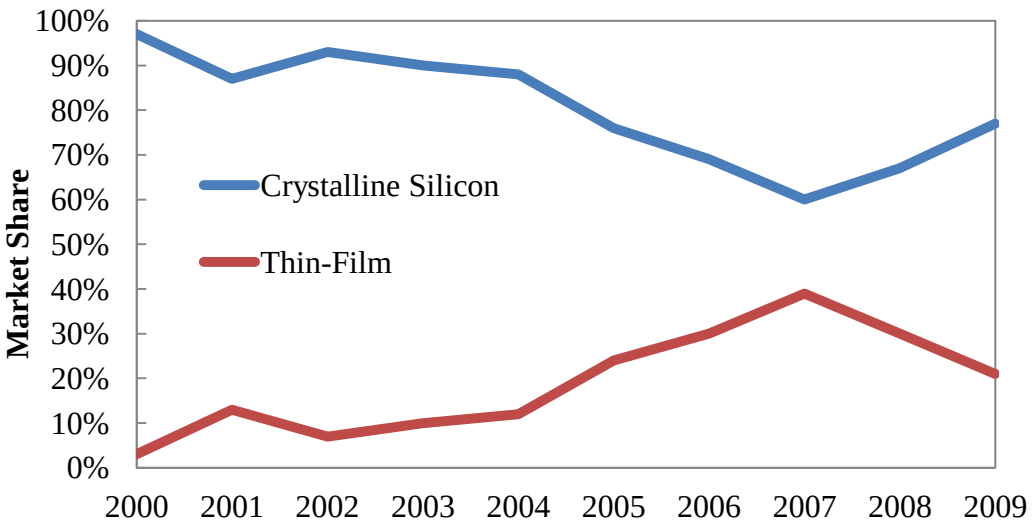


Figure 1.3: Crystalline Silicon and Thin-Film Market Shares in the U.S, 1999-2008 [3]

Lowering the cost of PV and increasing its production and implementation are part of the continuing quest to make PV technology achieve grid parity without the aid of subsidies, a target that could be reached in the next 5 years. Data from the US Department of Energy's multiyear program plan (MYPP) suggests that for PV to achieve a cost comparable to legacy utility providers, the cost of an installed residential PV system has to reduce to \$3-\$3.50/W_p from its current value of over \$4/W_p [4] in conjunction with module efficiency of 20%.The installed system cost includes balance of system (BOS) costs and the module cost. Prior work at Georgia Tech modeled requirements for the feedstock cost, cell efficiency, and balance of system costs that will result in grid parity in accordance with the MYPP [5]. It was found that cells produced on thin industrially viable materials would need to have efficiency ~20% at a price of ~\$1/W for this target to be reached, as seen in figure 1.4. Since the module price is already around \$1/W, the overall objective of this work is to provide technology solutions and roadmaps that

improve the cell efficiency from their current state of 16-18% to >20% to help achieve grid parity.

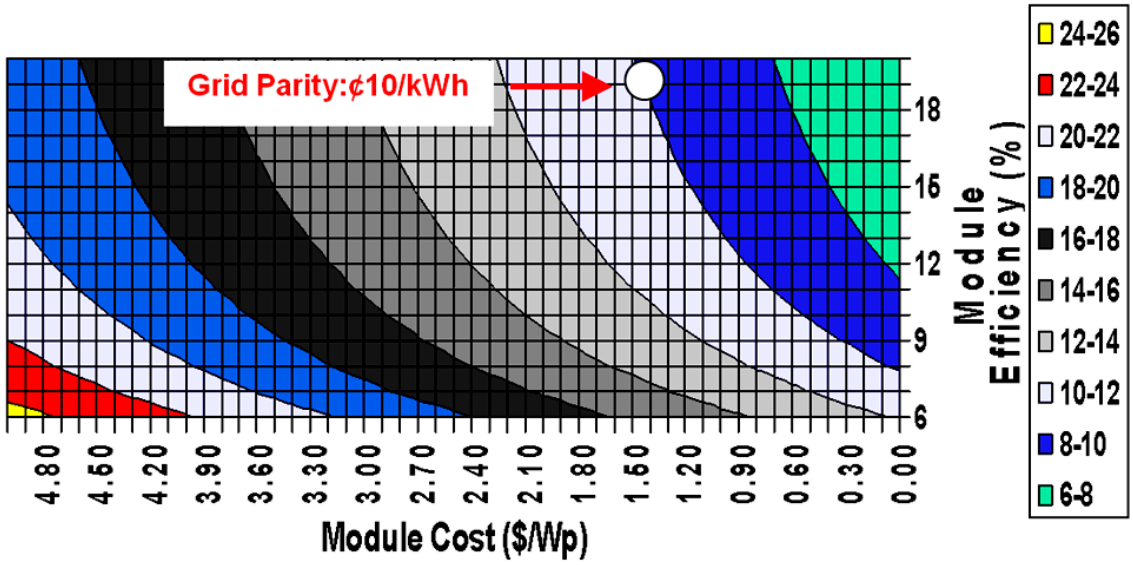


Figure 1.4: Cost analysis for achieving grid parity [4]

1.3 Objective of the study

The most commonly used cell design employed in the crystalline Si industry consists of cells with full aluminum back surface field (BSF) (Fig 1.5). Since the silicon raw material accounts for 40-60% of the total cost of a finished solar cell [6], it is important to reduce the Si wafer thickness. The use of lower grade Si feedstock can also contribute to some cost benefits as seen from the increasing use of multi-crystalline silicon substrates [7, 8]. However, thinner wafers have problems associated with wafer bowing and this affects yield. In addition, while the use of full BSF on cells provides moderate passivation, it sets limits on the maximum achievable efficiency by limiting back surface recombination

velocity and back surface reflectance. Progress towards higher efficiencies requires some critical changes in the cell design and manufacturing, both on the front and rear surface. Therefore, a roadmap was developed first with PC1D, quasi-one-dimensional finite-element program for modeling semiconductor devices [9]. This roadmap, seen in Figure 1.6, outlines the efficiency increase with each subsequent improvement while taking the manufacturability or the technology into consideration. Currently manufactured solar cells vary in efficiency and the best cells have addressed the specified improvements reaching efficiencies over 18%. As noted in the roadmap, there is nearly an increase in efficiency of ~1% (absolute) to be gained from improving the rear passivation and reflectance. An increase in cell efficiency of this magnitude has positive effects that propagate through the silicon value chain from material,manufacture to end-user. While this simulation uses high lifetime substrates, the modified technology can be easily adapted to commercial grade thin manufacturable materials without substantial loss in performance. This necessitates a move from the conventionally used simple cell design to a technology that involves improved surface passivation and rear internal reflectance. A more detailed look at these structures and their properties will be provided in subsequent sections.

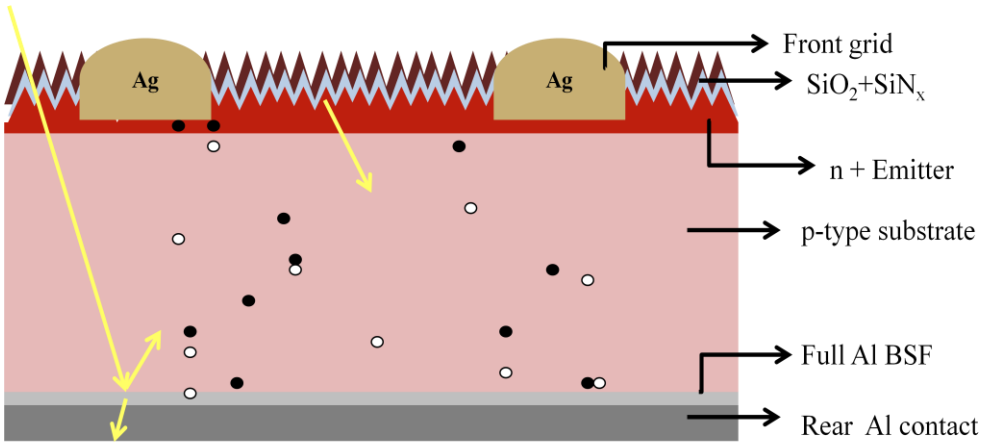


Figure 1.5: Schematic of a full Al BSF solar cell

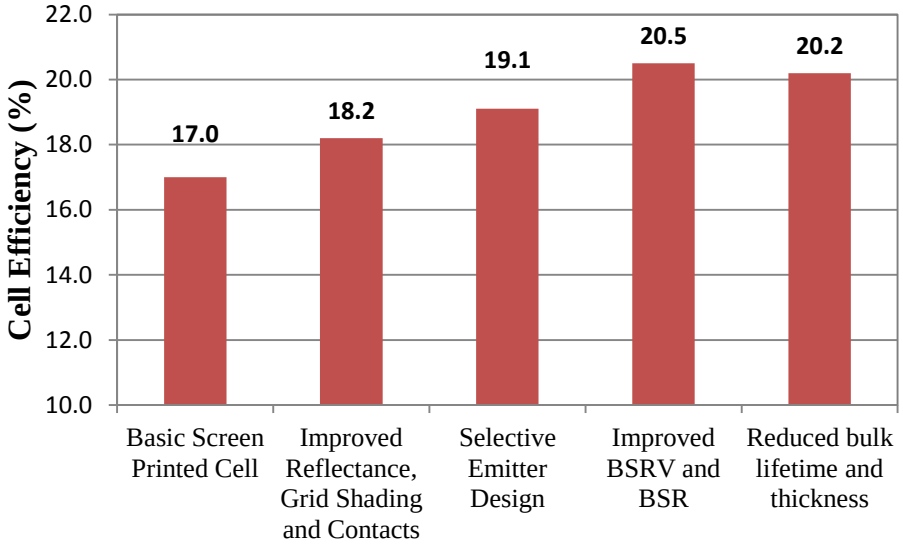


Figure 1.6: Roadmap to 20%-efficient c-Si solar cells with screen printed contacts

1.4 Specific Objectives

The overall goal of this research is to develop front and rear side technologies that can reduce FSRV and BSRV and increase BSR to boost Si solar cell efficiency by >1% (absolute) and drive its efficiency to ≥20%. This work consists of investigating a new cell design to produce high efficiency on thinner and cheaper substrates using spin-on

solutions. The use of lasers is also investigated to simplify cell fabrication and enhance throughput for industrial scale production. Owing to the availability of tools and equipment, 20% efficient cells will be fabricated on small area (4 cm^2) cells but the benefits of this technology advancement can be transferred to large area cells. Attempts will be made to develop cell designs and technologies that can be easily applied to thinner and larger cells without compromising efficiency in order to capture additional cost benefit from the technology innovation in this research. In order to accomplish this goal, this research has been divided into four tasks.

1.5 Task 1: Study and Optimization of a Phosphoric Acid Dopant Source

In this work novel cell structures are fabricated using spin-on solutions for emitter formation and rear diffusion. All prior work in the literature with commercial spin-on solutions has generally resulted in reduced process flexibility and reproducibility. As a result, one of the basic requirements for this research was to develop in-house phosphoric acid solutions that can serve as effective dopants and can be easily integrated into the process. Unlike most prior attempts that used tube or belt technologies, in this research, phosphoric acid is used as a limited source in tube diffusion processes. Phosphoric acid emitters were diffused under various conditions and analyzed. Emitters were diffused with phosphoric acid solutions of different concentrations at various temperatures to obtain the desired sheet resistance. Emitter profiles are also measured to ensure that it agrees with the required profile. The spin-on process was found to be sensitive to spinning conditions and process gas flow. Therefore, a better understanding of the mechanism of diffusion and dopant transfer was gained and applied to improve the

uniformity and quality of the emitter by including a "pre-oxidation" step in the diffusion process. Emitter saturation current density and profile measurements are performed to support that these emitters more suitable for high efficiency cells with screen-printed contacts.

1.6 Task 2: High efficiency cell fabrication using a spin-on phosphoric acid solution based emitter

In the previous task, suitable emitters were developed for high efficiency cells. In this task, complete cells are fabricated an analyzed to demonstrate its efficacy. Wafers were first diffused with emitters of different sheet resistances and simple baseline cells with full BSF were fabricated to evaluate their performance. In order to make good screen printed ohmic contacts, several front contact pastes (Ag) were tried to obtain high-aspect ratio gridlines and contact firing was optimized to reduce contact resistance. Based on these experiments an ideal combination of sheet resistance, paste and firing recipe was identified in this task. Previous work in the literature, including at UCEP, on full BSF cells with $POCl_3$ high sheet resistance emitters has resulted in a peak efficiency of 19%. However initial cells fabricated using spin-on phosphoric acid (PA) diffusion produced efficiencies of < 19%. This was traced to poor junction isolation using a dicing saw, which increased junction leakage and lowered fill factors (FF). Therefore a modified edge isolation process was devised in this task to isolate 4 cm^2 in a wafer. This resulted in high FF and a slight improvement in cell V_{OC} and J_{SC}, resulting in a record high 19.6% cell efficiency validated that spin-on phosphoric acid emitter can give high performance

cells. Detailed cell analysis of the 19.6% cell showed that the rear contact recombination has now become the limiting factor for cell performance. Therefore in the following tasks focus shifted to a high quality rear passivation scheme to attain the goal of ≥ 20% efficient screen printed cells.

1.7 Task 3: Development of a streamlined a spin-on solution based process for high efficiency LBSF cell design

Full BSF cells are the most common in the industry because they are easy to fabricate with relatively inexpensive methods. Novel cell designs with higher cell efficiencies require improved rear passivation technologies in combination with high quality front passivation. Various rear passivation schemes have been explored in the literature and some optimal candidates have been identified. Initial attempts were made in this task to fabricate cells with the high quality emitter with two different simple rear passivation techniques – thin and thick thermal oxides with a PECVD SiN_X cap. However both these structures resulted in cell efficiencies lower than full BSF cells due to parasitic shunting. Therefore a novel spin-on-dielectric based passivation scheme was developed and applied in this task to fabricate dielectric passivated local BSF (LBSF) cells. A streamlined process was developed in this task to combine the benefits of the high quality emitter and this rear passivation scheme. The unique and simplified process utilized only one high-temperature furnace step to diffuse an emitter and passivate front and rear surfaces. It was easily integrated with existing tools and methods to produce a peak cell efficiency of over 20%. These cells were characterized, in this task, to support the improved rear

passivation and rear internal reflectance expected from this LBSF structure. Some weaknesses are also identified in this task that need to be addressed before it can be used for commercial production.

1.8 Task 4: Comparative study of methods of laser ablation for rear-dielectric patterning for LBSF cells

To take advantage of the high quality passivation of the rear dielectric, parasitic shunting around the rear contacts needs to be avoided. The high efficiency cells described in the earlier section used screen-printing method to pattern vias through the rear dielectric for making local contacts. This method resulted in some non-uniformities in via definition which could affect the reproducibility of high efficiency cells and in the worst case result in efficiencies below those of a full BSF design. To circumvent this problem and render this technology less sensitive to process variations, substrate thickness and surface irregularities, laser ablation of rear vias was examination as an alternative in this task. Several laser candidates were identified – namely CO_2 laser (CW and pulsed), Near IR, UV and Green Laser. While peak cell efficiencies obtained from each process were comparable, when throughput and yield were considered, the UV laser was chosen. The processing using this laser was optimized for two different contact geometries resulting in peak efficiencies of 20.1% with the overall cell performance being comparable to the fully screen printed process. This confirmed that there had been no loss in passivation quality from the laser patterning. Further characterization of the cells was done using IQE

and SEM in this task to demonstrate that the formation of LBSF by laser is as good or better than the screen printed etching paste.

1.9 Task 5: Progress towards cost effective manufacturable solutions for LBSF Cz cell designs

In the previous tasks, 20.1% efficient device was achieved on 4 cm^2 float zone (FZ) silicon wafer through design, and implementation of a rear passivated local BSF device. Since Czochralski (Cz) Si is used in industry for monocrystalline cells, in this task, the novel LBSF technology was applied to Cz wafers to test its manufacturability and impact. Cz substrate generally has lower bulk lifetime, which can be compensated by using thinner wafers, which in turn will lower the silicon cost further. In this task, first simulations were performed using PC1D to calculate the expected peak efficiency when transferring this technology to thinner Cz substrates. Since this passivated cell design has a significant dependence on rear surface passivation, finish and smoothness, experiments were conducted to identify optimal single side planarization techniques for thin Cz materials. The surface with the least roughness was then used in cell fabrication on magnetically stabilized Cz (mCz) and regular Cz substrates. Cells were first fabricated on high bulk lifetime (>300 μs) thin mCz wafers and found to have cell performance comparable to that of thick FZ cells described in the previous tasks. Cells were then fabricated on lower lifetime (~ 200 μs) Cz substrates to see the effect of reduced bulk lifetime and thickness. Cz material is also known to suffer from light induced degradation (LID), which can be mitigated by lower Boron or higher substrate resistivity. Therefore,

in this task, effect of Cz substrate resistivity on passivation, LID and cell efficiency was also evaluated in an effort to determine optimum substrate resistivity.

CHAPTER 2

REVIEW OF BACKGROUND RESEARCH

2.1 Introduction

Research aimed at increasing cell efficiency requires an understanding of the fundamental operation of the solar cell and various deficiencies of the existing technologies. This helps to identify the regions that can be improved and to estimate the benefits from such improvements. In subsequent sections, three major areas are identified, which when addressed, are expected to increase cell efficiencies and bring PV technology closer to the target of grid parity, as discussed earlier. Some examples of other high-efficiency cell structures are also discussed which help to outline a path towards manufacturable cost efficient cell design.

2.2 Review of Recombination in Solar Cells

There are several factors, from atmospheric to microscopic, that result in a loss of efficiency in converting light energy to electrical energy in a solar cell. Some of these are systemic while others are particular to the cell design and fabrication techniques and can be minimized. One such loss occurs from the recombination of generated electron-hole pairs resulting in a significant loss of efficiency. A complete understanding of these phenomena is critical to optimizing high efficiency cell design and processing.

Fundamentally, electrical energy is produced in a solar cell when the energy from an incident photon creates an electron-hole pair in the bulk material of the solar cell. These carriers are separated at the junction and swept to surfaces where they are collected by the contacts towards the external circuit. The maximum benefit of this process is harnessed when all the carriers are safely collected at the metal contacts. However, there are several areas in the solar cell where these carriers can recombine with each other. The five main areas where this occurs in a simple single junction solar cell are listed below.

1. Front surface
2. Emitter
3. Depletion regions around the junction
4. Base
5. Rear surface

While all of these factors need to be studied for obtaining high efficiency, this work in particular deals with the reduced recombination at the surfaces and the emitter. The subsequent sections will look at recombination at the surface in detail while also providing methods to reduce this recombination.

Before discussing details and definitions of the types of recombinations, it is helpful to review some of the main quantities associated with recombination in solar cells.

1) Volume recombination rate, U ($cm^{-3}s^{-1}$) is defined as the rate of recombination of carriers per unit volume per unit time in the bulk of the material.

2) Carrier lifetime, τ (s), is defined as the average time spent by the carriers in the material before recombining.

Based on fundamental semiconductor physics, carrier concentrations are denoted n and p based on their type. At equilibrium carrier concentrations can be represented by the following equation

$$np = n_i^2 \tag{2.1}$$

where, n_i is the intrinsic carrier concentration of silicon, ~1×10^{10}.

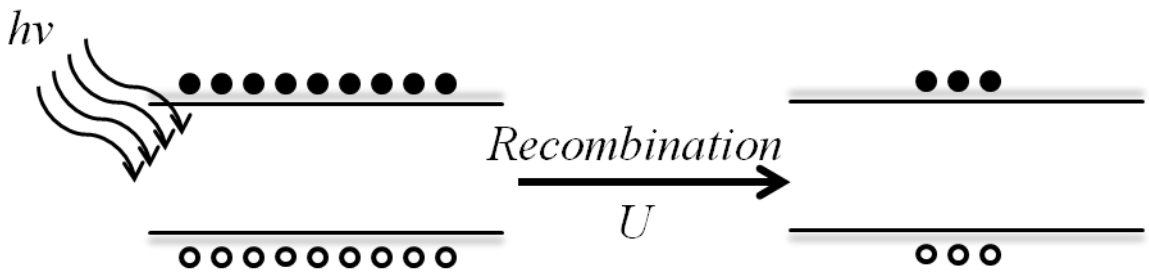


Figure 2.1: Schematic of generation and recombination of carriers in a material

As an effect of the incident light, the carrier concentrations are perturbed from equilibrium and can be denoted as,

$$np > n_i^2 \tag{2.2}$$

When the light is turned off, the carrier densities return to normal through recombination. The lifetime of the excess carriers in the material is dependent on the recombination rate and the excess carrier concentration by the equation

$$\tau = \frac{\Delta n}{U} \tag{2.3}$$

This equation is only valid in non-equilibrium conditions where excess carrier concentration can be expressed as a function of time and bulk lifetime.

$$\Delta n(t) = \Delta n(0) \exp(-t/\tau) \quad (2.4)$$

The excess carrier concentration is an important factor in studying the various types of recombination and their mathematical expressions. Based on this, two important injection carrier concentration regimes are identified for simplification of the analytical expressions. Low-level injection (LLI) is defined as the condition where the excess carrier concentration is smaller than the doping density of the semiconductor material by at least an order of magnitude.

$$\Delta n << N_a \text{ for LLI for a p type semiconductor} \quad (2.5)$$

High-level injection (HLI) is defined as the condition where the excess carrier concentration is larger than the doping density of the semiconductor material by at least an order of magnitude.

$$\Delta n >> N_a \text{ for HLI for a p type semiconductor} \quad (2.6)$$

Based on these primary definitions, analytical solutions for the physics of various types of recombination have been developed. The three main modes of recombination occurring in solar cells are listed below.

2.2.1 Band to band recombination

This is the type of recombination that occurs when an electron drops from the conduction band into the valence band directly and the resulting energy from this transition is released in the form of light as seen in figure 2.2. Hence it is also referred to as **radiative recombination**.

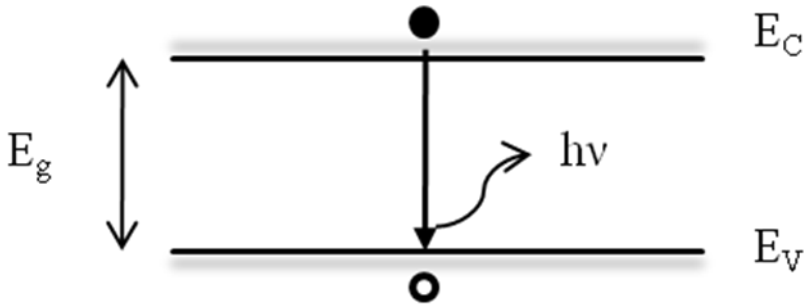


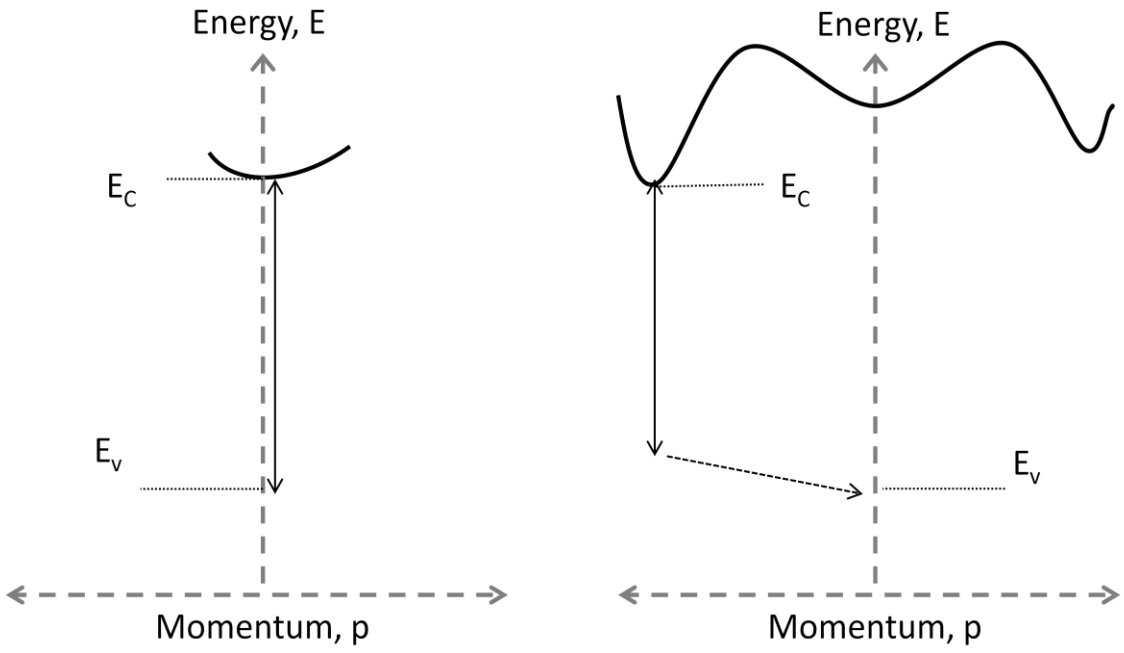
Figure 2.2: Schematic representation of radiative recombination

The relation between minority carrier lifetime and carrier concentrations as a result of band-to-band recombination is given as

$$\tau = \frac{\Delta n}{B.(n_0+\Delta n).(p_0+\Delta p)} \tag{2.7}$$

,where B is the coefficient of radiative recombination and n_0 and p_0 are free carrier concentrations at thermal equilibrium. For Si, B has a value of ~ 1.8×10^{-15} cm^3s^{-1} and for GaAs, B has a value of ~ 7.2×10^{-10} cm^3s^{-1}. This large difference in constants is because Si is an indirect band gap semiconductor while GaAs is a direct band gap material. In the case of an indirect band-gap semiconductor, there is momentum transfer to the crystal lattice, in the form of a phonon, in addition to the emission of radiation during recombination, as seen in figure 2.3. As a result, when comparing identically

doped materials using (2.7), Si will be found to have a minority carrier lifetime that is orders of magnitude higher than that of GaAs. Hence, in Si, this recombination doesn't play as important as role as the other types discussed in subsequent sections.



(a) (b)

Figure 2.3: Schematics of band-to-band recombination in (a) direct band gap and (b) indirect band gap semiconductors

HLI and LLI assumptions can be used to further simplify the expression for minority carrier lifetimes as follows.

$$\tau = \frac{1}{B.N_a} \qquad \text{at LLI} \qquad (2.8)$$

$$\tau = \frac{1}{B.\Delta n} \qquad \text{at HLI} \qquad (2.9)$$

,where N_a is the doping density of a p-type substrate. In summary, one can observe that radiative recombination has a small but constant effect at low injection levels and its effect continues to reduce as injection level increases.

2.2.2 Auger recombination

This is the form of recombination where other than an electron and hole interacting to recombine, the excess energy is transferred to another electron or hole, hence altering its energy state. It can be considered to be the inverse effect of impact ionization. A schematic representation of this can be seen in figure 2.4. As a result, there is no emission of radiation in this mode. This mode of recombination requires carriers in close proximity to one another and hence, is particularly relevant in high level injection and highly doped regions. For example, auger recombination is very active near the surface in the emitter region of a solar cell where there is a high density of dopant atoms. A well designed emitter should have low auger recombination resulting in a better cell performance.

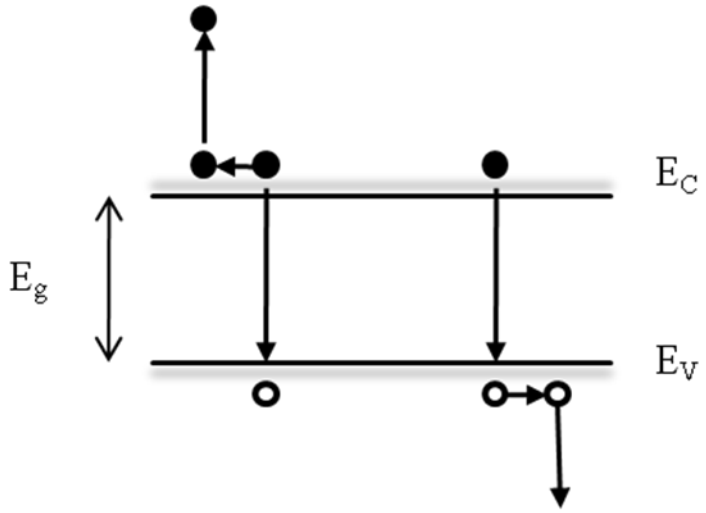


Figure 2.4: Schematic representation of Auger recombination

Auger recombination rate is defined as

$$U = C_n \cdot n^2 \cdot p + C_p \cdot p^2 \cdot n \quad (2.10)$$

,where C_n and C_p are the Auger recombination coefficients for electrons and holes, respectively. Using this and the assumptions for injection level, the following expressions for carrier lifetime as a result of Auger recombination can be defined.

For p-type: $\tau = \frac{1}{C_p . {N_A}^2}$ at LLI and $\tau = \frac{1}{(C_p + C_n) . \Delta n^2}$ at HLI (2.11)

As seen from these expressions, carrier lifetime is inversely related to the second order of carrier concentration, while band-to-band recombination was had a linear relation. Hence, Auger recombination has a much stronger effect on lifetime. Also it can be seen that as injection level increases, the effect of Auger recombination on lifetime continues to get stronger.

2.2.3 Shockley-Read-Hall recombination

This is the form of recombination that occurs at defects, surfaces and other interfaces. These provide intermediate energy levels within the band gap providing a suitable transition point for the electrons to transition into before falling into the valence band as seen in figure 2.5. This phenomenon was studied and explained in detail by Shockley, Reed and Hall and hence is commonly referred to as Shockley-Reed-Hall recombination (SRH) [10,11]. This is a dominant mode of recombination in lower lifetime materials and at surfaces owing to an increased availability of defect and impurity related energy states.

Controlling this mechanism of recombination is vital to achieving good surface passivation, resulting in a better cell performance. Various methods of achieving this will be analyzed in the subsequent sections.

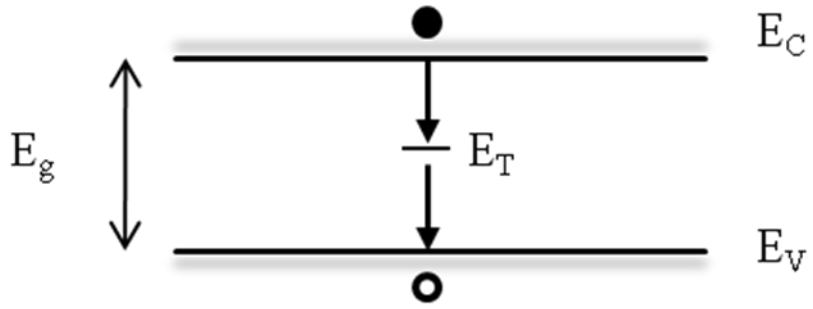


Figure 2.5: Schematic representation of SRH recombination

Some important assumptions are made for the derivation of analytical expressions explaining this type of recombination [12]. These are listed below.

a) Radiative and Auger recombinations are ignored

b) Non-degeneracy of the semiconductor material is assumed

c) The energy level of the defects is not affected by their charging properties

d) Fermi-Dirac statistics are applicable

e) Transitioning carriers only interact with one intermediate level and hence each trap level is considered to be unaffected by other trap levels

f) Time spent by carriers in the trap level is negligible

Based on these assumptions, the SRH recombination rate is defined as

$$U = \frac{(pn - n_i^2)}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{2.12}$$

,where τ_{n0} and τ_{p0} are characteristic carrier lifetimes related to the thermal velocity of the carrier, υ_{th}, the defect concentration, $N_{t,}$, and the capture cross-sections of carriers for the defect, σ. The mathematical relations for τ_{n0} and τ_{p0} are as follows:

$$\tau_{p0} = \frac{1}{\sigma_p N_t \upsilon_{th,p}} \quad \text{and} \quad \tau_{n0} = \frac{1}{\sigma_n N_t \upsilon_{th,n}} \tag{2.13}$$

p_1 and n_1 are defined as the free carrier concentrations in the condition at which the Fermi energy level (E_F) coincides with the trap energy level (E_T). The mathematical expressions for calculating them are

$$p_1 = n_i exp\left(\frac{E_{i-} E_T}{kT}\right) \quad \text{and} \quad n_1 = n_i exp\left(\frac{E_{T-} E_i}{kT}\right) \tag{2.14}$$

Using 2.12 and the basic expression for calculating lifetime, SRH lifetime can be expressed as

$$\tau_{SRH} = \frac{\tau_{p0}(n+n_1)+\tau_{n0}\,(p+p_1)}{n_0+ p_0+\Delta n} \tag{2.15}$$

Expressions for SRH lifetimes under various conditions can be derived by making the appropriate approximations.

For p-type Si in LLI, $p_0 >> n_0$, Δn, Δp

$$\tau = \tau_{n0}\left(1 + \frac{p_1}{p_0}\right) \tag{2.16}$$

and in HLI , $\Delta n >> p_{0,}\, n_{0,}\, p_{1,}\, n_1$

$$\tau = \tau_{n0} + \tau_{p0} \tag{2.17}$$

When the material has deep trap levels, it is a reasonable approximation to assume that $E_T \approx E_i$. As a result both n_1 and p_1 are equal to n_i and negligible when compared to p_0. This reduces the expression for lifetime of a p-type Si with mid-gap traps at LLI to

$$\tau = \tau_{n0} \tag{2.18}$$

On examining the analytical solutions for SRH lifetime at various conditions, it can be noted that at low level injection, the carrier lifetime depends on all the defect parameters – defect energy, capture cross-section and defect concentration. However, in high level injection, the absence of an "n_1" term in the expression indicates that lifetime is not affected by the energy of the trap level. It can also be noted that the lifetime is lowest with mid-gap traps and is limited by minority carrier capture. As a result, traps that lie at the middle of the band gap are the most harmful for material lifetime and cell performance and have to be minimized.

In practice all of these factors act simultaneously and the net recombination in the bulk of the material is a sum of all individual factors, as seen in figure 2.6. The net lifetime (τ_{net}) can therefore be expressed as follows:

$$\frac{1}{\tau_{net}} = \frac{1}{\tau_{BB}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \tag{2.19}$$

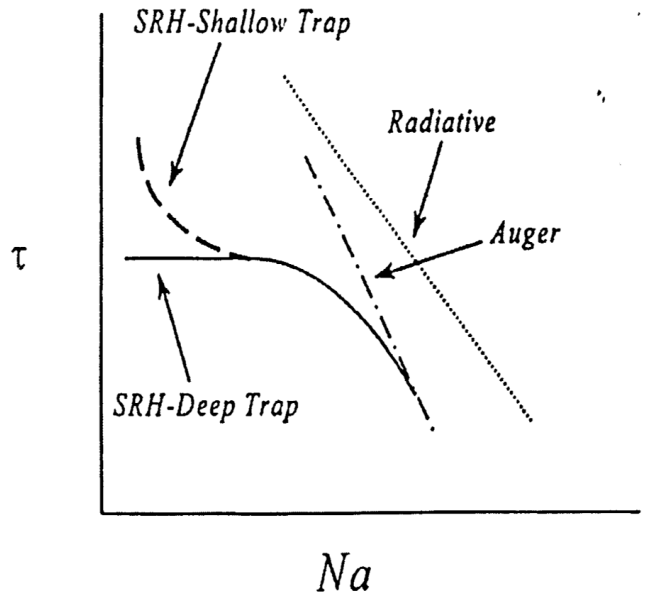


Figure 2.6: Schematic representing the individual trends of various forms of recombination and their combined effect on net material lifetime

2.2.4 Surface Recombination

Surfaces of materials mark an end of the periodicity of atoms and bonds and hence, offer a high density of defects and imperfections in the form of dangling bonds. These offer energy levels for recombination and as a result are a critical feature of solar cells that need to be controlled to achieve good device performance. Surface recombination proceeds through intermediate energy levels provided by surface defects as seen in figure 2.7. The physics of SRH recombination apply to it, but with some modifications. As this thesis deals with a high efficiency surface passivated device, a brief overview of the theory behind this recombination phenomenon is provided in the following section.

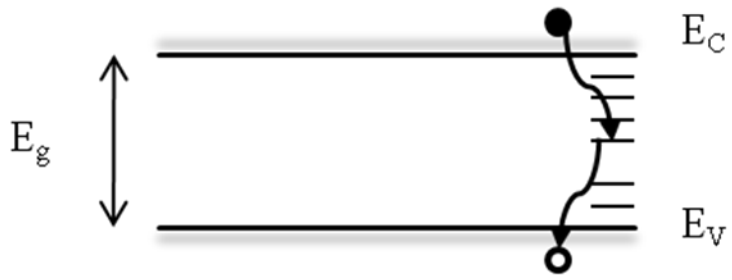


Figure 2.7: Schematic representation of surface recombination

Most of the parameters used in SRH recombination apply to surface recombination. A new parameter referred to as surface recombination velocity (S or SRV) is added which is unique to this phenomenon. This parameter bears the physical dimensions of speed and can, hence, be referred to as the velocity of excess carrier flow to the surface. This parameter provides a rate of recombination of carriers at the surface per volume of excess carriers and can be defined as follows:

$$S \equiv \frac{U_s}{\Delta n} \tag{2.20}$$

Replacing some parameters from the SRH formulation with surface specific quantities, a simple formula for the rate of surface recombination can be obtained as

$$U_s = \frac{S_{p0} S_{n0} (n_s p_s - n_i^2)}{S_{n0}(n_s + n_1) + S_{p0}(p_s + p_1)} \tag{2.21}$$

,where n_s and p_s are carrier concentrations at the surface. S_{n0} and S_{p0} are characteristic surface recombination velocities related to the density of surface states (N_{st}), capture cross sections and thermal velocities as

$$S_{p0} = N_{st}\sigma_p \upsilon_{th} \quad \text{and} \quad S_{n0} = N_{st}\sigma_n \upsilon_{th} \tag{2.22}$$

When the characteristic surface recombination velocities are replaced with their expansions in equation (2.21), SRH recombination can be expressed as follows:

$$U_s = \frac{N_{st}\upsilon_{th}\left(n_s p_s - n_i^2\right)}{\frac{(n_s + n_1)}{\sigma_p} + \frac{(p_s + p_1)}{\sigma_n}} \tag{2.23}$$

While this equation expresses SRH at a specific surface state, to obtain the recombination as a result of all the energy levels at the surface, equation (2.23) has to be integrated across the entire energy gap. This results in a composite expression for surface recombination.

$$U_s = \left(n_s p_s - n_i^2\right) \int_{E_V}^{E_C} \frac{\upsilon_{th} D_{it}(E) dE}{\frac{(n_s + n_1(E))}{\sigma_p(E)} + \frac{(p_s + p_1(E))}{\sigma_n(E)}} \tag{2.24}$$

,where D_{it} is the density of interface states at each energy level per unit area.

From equation (2.24) it should be noted that surface recombination is proportional to two parameters that can be controlled through fabrication and design, namely carrier concentrations at the surface and the density of interface states. There are two main ways of reducing SRH recombination at the surface. The two main methods deal with different ways of reducing the availability of these conditions to reduce recombination as follows.

2.2.4.1 Introduction of dopants near the surface to control the carrier transport to the surface

This is the method of passivation that involves the use of a back surface field (BSF) or a floating junction near the rear surface to repel one type of carriers, while aiding the collection of the majority carriers. This might be achieved by way of either diffusion (eg. Boron BSF) or firing of the contact metal (eg. Al BSF). The most common type of crystalline silicon solar cells employs a full Al BSF on the rear for passivation and rear metal contact. A similar effect can also be obtained by the use of field effect passivation caused by the fixed charges in dielectrics such as SiO_2 and SiN_X films.

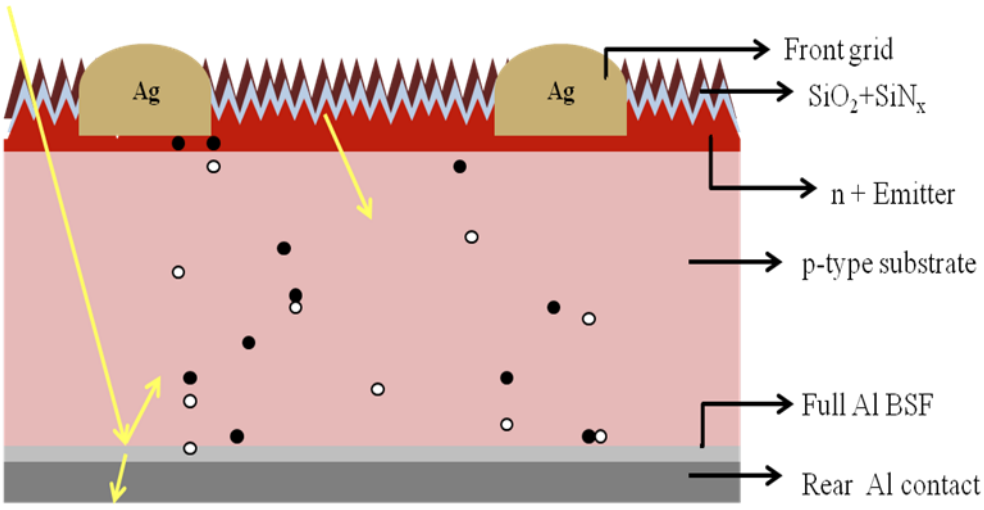
2.2.4.2 Surface passivation using dielectrics

As with any material surface the abundance of dangling bonds at the silicon surface provide trap levels that aid the SRH recombination. Effective surface passivation using dielectrics involve the elimination of most of these trap levels, thereby reducing the probability that electrons and holes will recombine even if they both reach the surface. This type of passivation has been attempted using several different dielectrics such as thermal oxide, PECVD SiNx and some other newer alternatives like amorphous Si (a-Si). A more detailed look at structures benefiting from this passivation technique will be provided in subsequent sections.

2.3 Overview of rear passivation

Conventional cell designs employing the full Al BSF technology have a back surface recombination velocity (BSRV) generally higher than 250 cm/s. This high value of BSRV is one of the main limiting factors in the efficiency of solar cells. Typical values of

recombination velocities for a metal directly in contact with the silicon surface can be $>1\times10^5$ cm/s. In addition a full BSF cells also have low back surface reflectance (BSR), with typical values less than 75%. A LBSF cell is a substantial improvement compared to full BSF structures. A high percentage of the rear surface is passivated with a dielectric. This contributes electrically and optically to improvements in cell performance. The two structures are seen in Figure 2.8. There are various dielectrics that have been long studied for passivation of the front and rear surfaces [13, 14]. The most common dielectric used in the PV and semiconductor industry has been a thermal SiO_2, which has several advantages when used on crystalline silicon substrates. The relative ease of growth of SiO_2 on silicon at high temperatures and the high-quality low-stress interface between the Si and the oxide are reasons for early adoption in the PV industry. The subsequent sections will provide an overview of the various types of oxides and their applications for solar cell passivation.



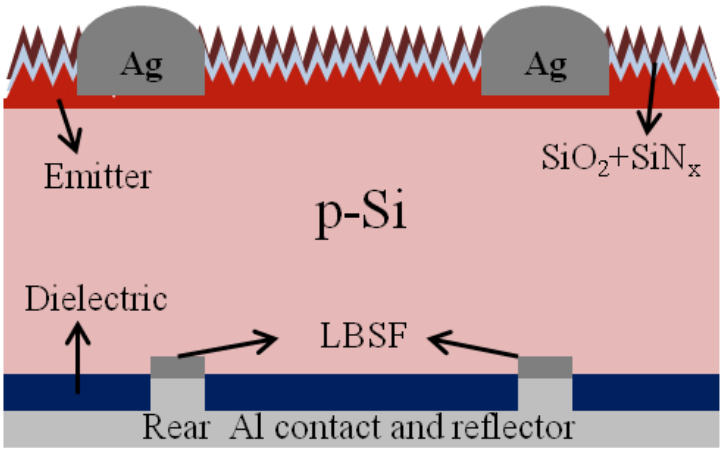


Figure 2.8: Schematics of full BSF and LBSF cell structures

2.4 A Review of Dielectric-Passivated Solar Cells

In any material, the surfaces are considered the most imperfect region. Hence dielectric passivation is considered to be a key component of reducing recombination at the surface of silicon to achieve the maximum performance of a solar cell. Dielectric passivation of solar cells has been known to be a path to high efficiency for decades leading to several designs being studied. The earliest crystalline silicon solar cells with efficiency exceeding 20% were fabricated at the University of New South Wales. These were known as the PERC and PERL cells [15, 16]. They both employed an identical front side textured with inverted pyramids and passivated with a thick oxide. While the PERL cell employed a locally diffused Boron BSF, the PERC cell achieved the high efficiency with just a local contact structure. One of the keys to these cells structures achieving efficiencies over 20% was the high quality passivation achieved by a thick thermal oxide, on the front and back, along with high internal reflectance. The low reflectance of the front surface was

achieved by a uniform inverted pyramid texture and a thick oxide was used as the anti-reflection coating. A good rear internal reflectance was a result of the evaporated Al on top of the passivating oxide. The PERL cell had a BSRV ~60 cm/s and BSR > 96% while the PERC cell had a higher BSRV of ~200 cm/s and a BSR of 95%. This combination resulted in cell V_{OC} exceeding 680 mV and J_{SC} exceeding 40 mA/cm^2. As seen in figures 2.9 and 2.10, these structures were highly complex involving several photolithography steps rendering them impractical for large scale production. Of these two cells, the PERC structure is simpler owing to the lack of a rear Boron diffusion and has become a template for simpler cell structures with modified processing methods. The PERL cell is however more robust to variations in contact geometry, substrate resistivity and dielectric charge owing to the locally diffused B regions under the rear contacts. These cells opened the way to high efficiency PV technologies and displayed the potential of crystalline PV and remain the highest efficiency single junction cells fabricated on crystalline Si.

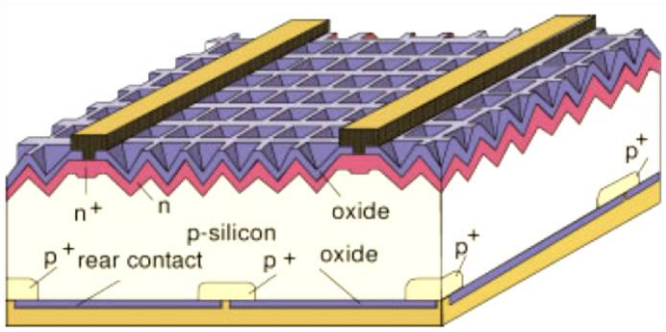


Figure 2.9: Schematic of PERL cell

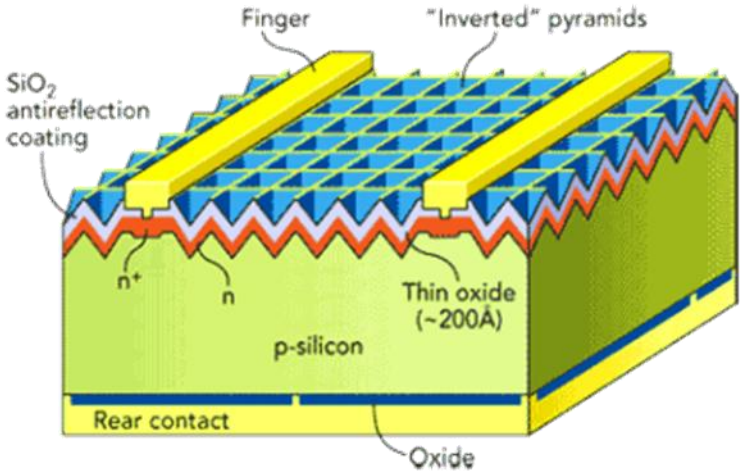


Figure 2.10: Schematic of PERC cell

The most common dielectrics used in the PV industry remain the oxide and SiNx for the reason that they are highly compatible with the existent processes and equipments.

2.4.1 Rear passivation using silicon nitride

PECVD SiN_x coatings were one of the earliest dielectrics of choice for passivating a silicon surface as they can perform the dual role of front surface passivation and anti-reflection coating. As they were already integrated into solar cell processes, SiN_x coatings were one of the options considered for high quality passivation of the rear surface in high efficiency solar cell designs. Typical high efficiency cells at that time were fabricated with thick thermal oxides as the rear passivating dielectric. These came at the expense of long, high temperature processes that affected the cost and throughput. At times these processes can also severely degrade bulk lifetimes which are undesirable. PECVD SiN_X provided an alternative low-cost effect surface passivation alternative. Initial experiments to characterize SiN_X coatings on a silicon surface revealed that a basic PECVD SiN_X can

provide a very high quality passivation [17]. Very low surface recombination velocities were recorded on low resistivity materials typically used for high efficiency cell processing [18]. This was due to two critical properties of PECVD SiN_X films. First the hydrogen released from these films helped passivate the dangling bonds at the surface, thereby reducing the interface state density. And secondly, PECVD SiN_X typically has a high positive charge in the dielectric and this attracts all the electrons towards the Si-SiN_X interface, thereby inverting the silicon immediately next to the interface. This reduces the availability of recombination centers near the surface and provides the high quality surface passivation. This type of passivation is called field effect passivation as it is achieved by an induced electric field because of the dielectric.

On fabrication of local BSF cells using SiNx rear passivation, it was observed the cells had high cell V_{OC} of up to 675 mV, confirming the high quality rear passivation comparable to cells with high temperature thick thermal oxides used for rear passivation [19-21]. However, cell J_{SC} and hence efficiencies were lower by more than 1% absolute when compared to the thermal-oxide passivated reference cells. After further characterization and analysis, this loss in current was attributed to the high fixed charge in the SiN_x. The negative effect of this type of passivation is the possibility of inverting the silicon surface by band bending near the interface. In the case of SiN_X films, this inversion is very strong and can lead to parasitic flow of electrons laterally between the rear contacts and the inversion layer. This parasitic shunt can result in cells with, low J_{SC} and FF and make the passivation appear bad. The magnitude of this parasitic shunt is

dependent on the injection level of rear surface, but in the case of strong inversion caused by SiN_X, the injection level reaches a high enough level to eliminate the parasitic shunt. Varying the silicon to nitrogen ratio in SiN_X films is one way of modifying the quality of the rear passivation. Measurements have been made to calculate the sheet resistance of the inversion layer formed under the dielectric and the effect of the film's refractive index on it [22]. A higher sheet resistance combined with effective surface passivation would reduce this effect. As seen in figure 2.11, minimum values for the sheet resistance are found when the refractive index is between 1.95 and 2.20. For lower refractive indices, the sheet resistance increases. This occurs with an increase in interface state density since the surface passivation decreases with decreasing Si content in the film. For higher refractive indices, the surface passivation is usually better as the increased sheet is caused by a decrease in fixed charge densities. Sensitivity to index is higher for lower substrate resistivities. Hence, for industrial situations the index would need to be carefully optimized. Ideally, very Si-rich SiN_X coatings are preferred for rear passivation.

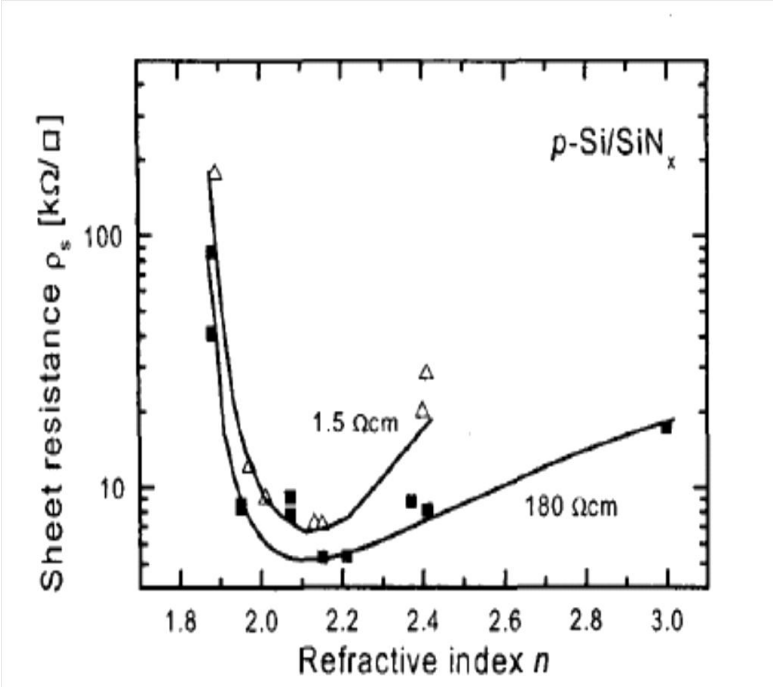


Figure 2.11: Measured sheet resistance of the inversion layer at the silicon surface as a function of refractive index of the SiN_X films on top of the silicon [22]

2.4.1.1 Characterization of SiN_x Rear Passivation

During characterization of these cells, this phenomenon can be observed by measuring the internal quantum efficiency (IQE). Cells with SiN_X passivation that have a low efficiency are found to have an artifact in the long wavelength IQE response (900nm - 1100nm) as seen in figure 2.12 [23]. With certain other types of field effect passivation, this signature of parasitic shunting at long wavelengths disappears with the use of a light bias (> 0.3 suns) when measuring IQE. In these cases, the injection level dependence of the inversion is such that at cell operating conditions, the injection level eliminates the parasitic shunt leading to very low surface recombination and high cell efficiency. In this

thesis, one such combination is used for rear surface passivation in fabrication of a high efficiency solar cell.

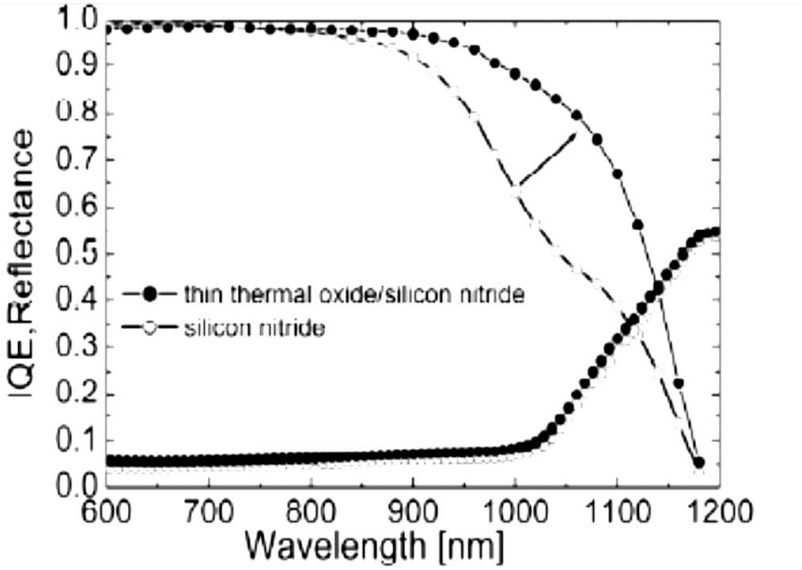


Figure 2.12: Internal quantum efficiency and reflectance measurement of high-efficiency silicon solar cells with textured front. The loss in J_{SC} due to parasitic shunting disappears when thin oxide is applied underneath the nitride

Another important characterization technique used to identify the effect of parasitic shunting is the use of dark I-V measurements [24]. When plotting the dark I-V curves, cells with field-effect passivation where a high positive charge is involved, have signature shoulders in the curves. Dark I-V data can then be processed and plotted as local ideality factor curves as seen in figure 2.13. The negative slopes of the curves can be calculated at each point – known as local ideality factor - and plotted against the sweep voltage [25]. Depending on the type of dielectric used for rear passivation, the shoulders manifest themselves as very clear signatures in the local ideality plots [26]. Typically SiN_X passivated cells show a bump around 570 mV while a SiO_2/ SiN_X stack

passivation scheme results in a lower bump at voltages around 500 mV. A thermal oxide passivated device displays no bump in the local ideality curve. The size and location of these signature curves can be related to the extent of inversion caused by each dielectric and thereby, qualitatively related to the parasitic losses in the device.

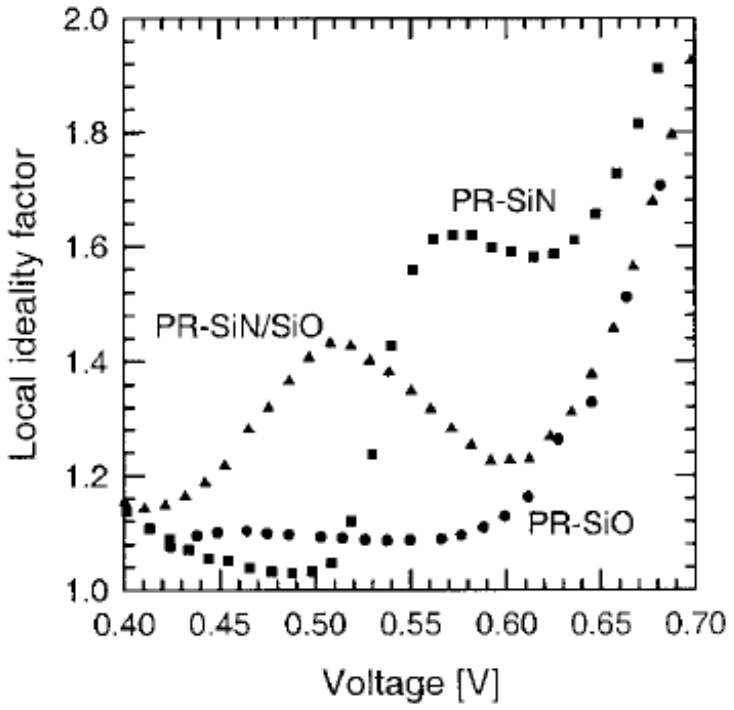


Figure 2.13: Local ideality factor–voltage (nloc–V) curves measured for SiO_2 passivated (circles), SiN_X passivated (squares), SiN_X/SiO_2 stack passivated(triangles) cells

Alternate methods have been suggested where a well doped BSF or an isolation ring with different passivation can be used to keep the rear metal contacts physically separated from the inversion layer to harness the maximum potential of SiN_X passivation. These studies have resulted in cell efficiencies of >20% [27]. However these methods are not compatible with low-cost high throughput processes and are hence, not considered for commercial use.

This injection level dependence of SIN_X passivation is analogous to the inversion observed in passivated emitter rear floating p-n junction (PERF) cells [28]. PERF cells achieve a high quality rear passivation by the diffusion of phosphorous on the rear surface. The floating junction is isolated from the contacts by means of a locally diffused BSF under the contacts. It was found that the cell performance was related to the sheet resistance floating junction or the distance between contacts [29] – an effect very similar to that discussed earlier with SiN_X passivation. As the doping level was increased or distant between contacts was decreased, an increase in parasitic loss of cell efficiency was observed. On characterization of these cells, it was observed that the parasitic effect had characteristic features in dark IV measurements (as seen in figure 2.14), local ideality measurements (figure 2.15) and, as with the SiN_X passivation earlier, a light bias dependence during IQE measurements.

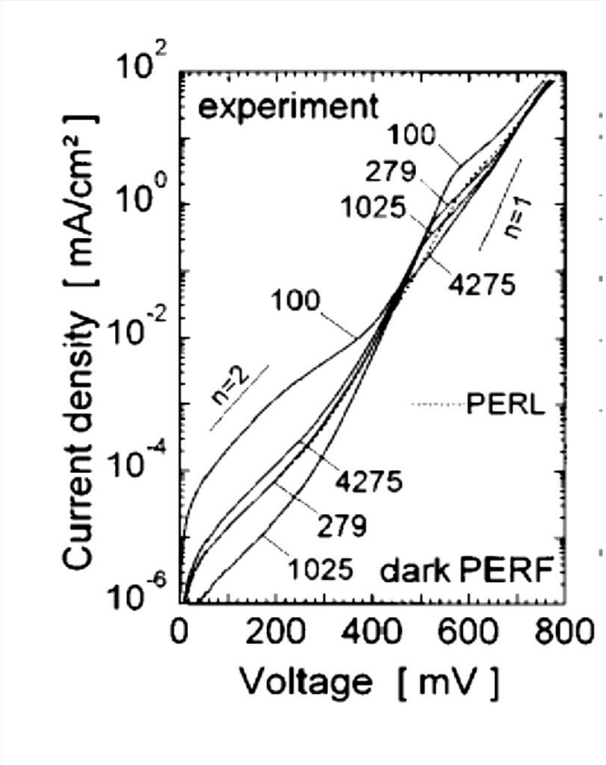


Figure 2.14: Measured dark I-V curves of the PERF cells investigated in [29]. The numbers refer to the sheet resistivity of the floating junction in Ω/□. The dotted line is the I-V curve of the PERL cell that was processed alongside the PERF cells

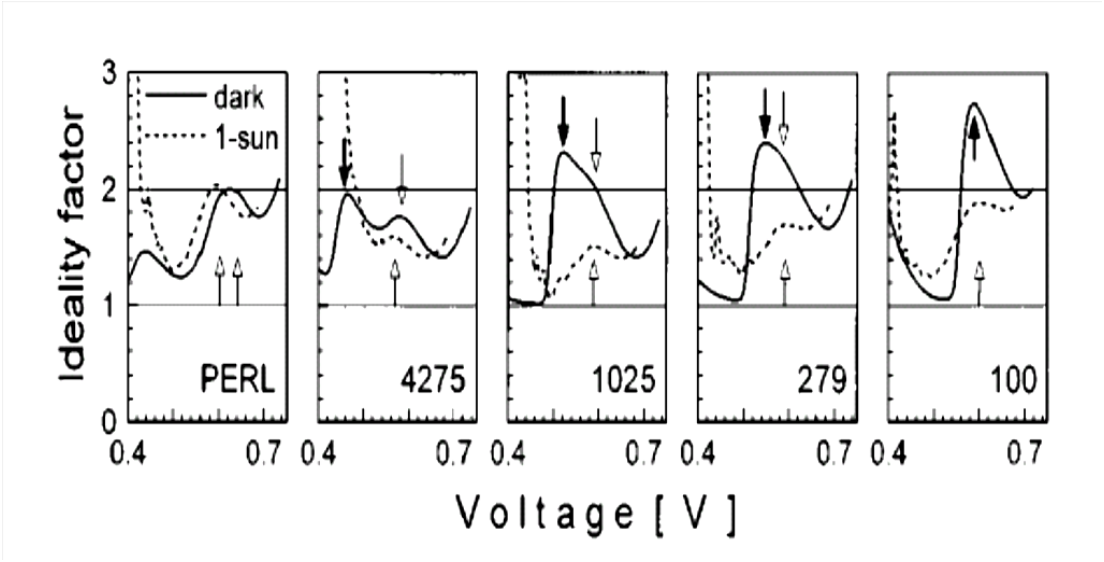


Figure 2.15: Local ideality factor of the experimental I-V curves of figure 2.14. The arrows indicate shoulders and the numbers refer to the sheet resistance of the floating junctions

This phenomenon can be simply explained as the effect of the forward bias potential across the p-n junction around the rear contact. This bias can be affected by the incident light reaching the rear surface. At high enough injection levels, the bias across the rear p-n junction is high enough that the effect of parasitic shunting is negligible and a very low BSRV is achieved. This dependence on injection level is observed as the cell is swept from V_{OC} to J_{SC}, which is why the kink in the long-wavelength IQE disappears under light bias. In extreme cases, when the rear sheet resistance is too low (~100 Ω/sq), the rear p-n junction never reaches a significant forward bias to minimize shunt losses and hence the device acts as a solar cell with poor BSRV.

A more detailed explanation of this phenomenon involves recombination mechanisms. Based on measurements of the properties of interfaces, it has been proposed that the very strong injection-level dependence is related to the large difference in the capture cross sections of electrons and holes ($\sigma_n/\sigma_p \approx 100$ near midgap) [30]. As injection level increases, the recombination at the rear surface transitions from being limited by the capture by minority carriers to being limited by capture of majority carriers. And since capture cross sections of holes are much lower, at higher injection levels, a far lower SRV is obtained.

Various practical issues with cell fabrication ensure that SiN_x passivation for high efficiency devices are not a feasible solution. Instead, the most common dielectric used for rear surface passivation in high efficiency laboratory and commercial devices, is SiO_2 and its various forms. SiO_2 also provides passivation using a milder form of field-effect

passivation and since this thesis deals with a form of SiO_2 passivation, a more detailed analysis of it is provided in subsequent sections.

2.4.2 Rear Passivation with Silicon Oxide

Different types of oxides have been studied for rear passivation, namely the classical thermal oxide (CTO), rapid thermal oxide (RTO) and the PECVD deposited oxide in combination with the conventional PECVD SiNx [31]. There is also an ongoing research in the use of wet oxides for rear passivation. The advantage that wet oxides have over CTO and RTO is that a thicker oxide can be obtained at a lower temperature and they grow quicker than dry oxides owing to a different growth mechanism [32, 33]. The reason for this can be explained using the following equations.

$$Si + O_2 \leftrightarrow SiO_2 \tag{2.25}$$

is the chemical reaction defining what happens during the formation of a dry CTO, while in the case of a wet oxide, the following reaction occurs between the Si wafer and the steam

$$Si + 2H_2O \leftrightarrow SiO_2 + 2H_2 \tag{2.26}$$

The oxidizing molecules need to travel through the already grown oxide to react with the Si at the surface to form a new oxide. As H_2O is a smaller molecule than O_2, it is able to travel to the Si/SiO_2 interface faster and hence grow a thicker oxide easier. As a result, this oxide is less dense and might not be suitable for all applications. However in the case of rear passivation it has been shown that the quality of this oxide is comparable to a

thick CTO, leading to a significant decrease in the thermal budget of this technology. Cell efficiency exceeding 19% on float zone substrates have been demonstrated with the use of wet oxide rear passivation [34]. The cell structure is simpler with random pyramid front texturing and hot-melt screen printing technology aided by light induced plating. The main advantage of this structure is the use of a laser to fire the rear Al in a precisely selected geometry to form local BSF, thereby obtaining a high quality passivation with a BSRV of <150 cm/s and a high BSR of 94%. A schematic of these laser fired contact (LFC) cells can be seen in figure 2.16. A slightly modified version of this structure employing the use of aerosol jet printing and light induced plating for front contacts increased the efficiency to over 20% [35]. This helps to achieve finer lines with high aspect ratio for the front grid, thereby reducing the average FSRV, while making no changes to high quality rear passivation. This resulted in cell V_{OC} over 660 mV with a high fill factor over 80%. The manufacturability of these cells is better than the aforementioned PERL and PERC cells, but the front metallization schemes used in these devices are not yet embraced for production on an industrial scale. Simpler devices using the conventional screen printing technology and wet oxide/PECVD SiO stack for rear passivation have been demonstrated on larger cells (>149 cm^2) with efficiency over 18.0% [36].The schematic of this cell design, referred to as a SiNTO cell, can be seen in figure 2.17. Additional modifications to this design have resulted in screen printed cell efficiencies of over 19.5 % on larger Cz substrates (239 cm^2) [37, 38, 39]. These results represent some of the state-of-the-art devices which demonstrate the advantages of using oxide rear passivation.

However there are issues associated with using oxides for rear passivation. There are some questions about the thermal stability of oxide only dielectrics. Quite often they are used in combination with a cap – PECVD oxide or SiNx - in order to preserve the passivation quality during contact firing. Thermal oxides come with an inherent positive charge and so do nitrides. The magnitude of the charge may vary based on the method and the furnace used but in general the charges are high and positive in nature. While these charges are beneficial, in effect providing a field effect passivation of the rear surface, they come with a possibility of loss of cell performance through parasitic shunting. As a result the cell fabrication has to be specifically tailored to eliminate shunts and retain the benefits of the high positive charge of the dielectric.

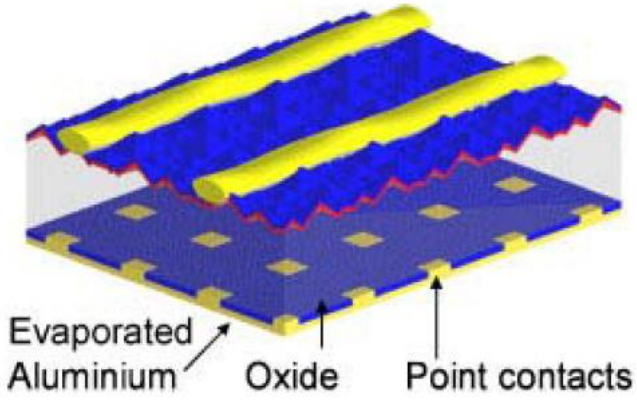


Figure 2.16: Schematic of cell structure with laser fired rear contacts

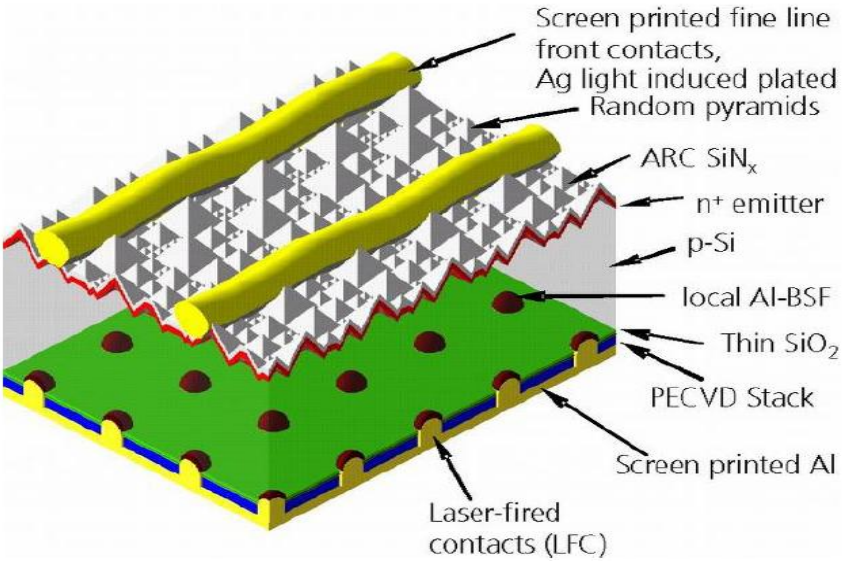


Figure 2.17: Schematic of SiNTO cell structure with laser fired rear contacts

2.4.3 Alternate Dielectrics for Rear Passivation

An alternative to the using thermal oxides and dealing with the parasitic issues is to use other dielectrics which inherently possess a high negative charge. A good quality dielectric with a high negative charge is known to produce cell performances as good as a good thermal oxide. The results of preliminary modeling to study these effects can be seen in figure 2.18 [40].

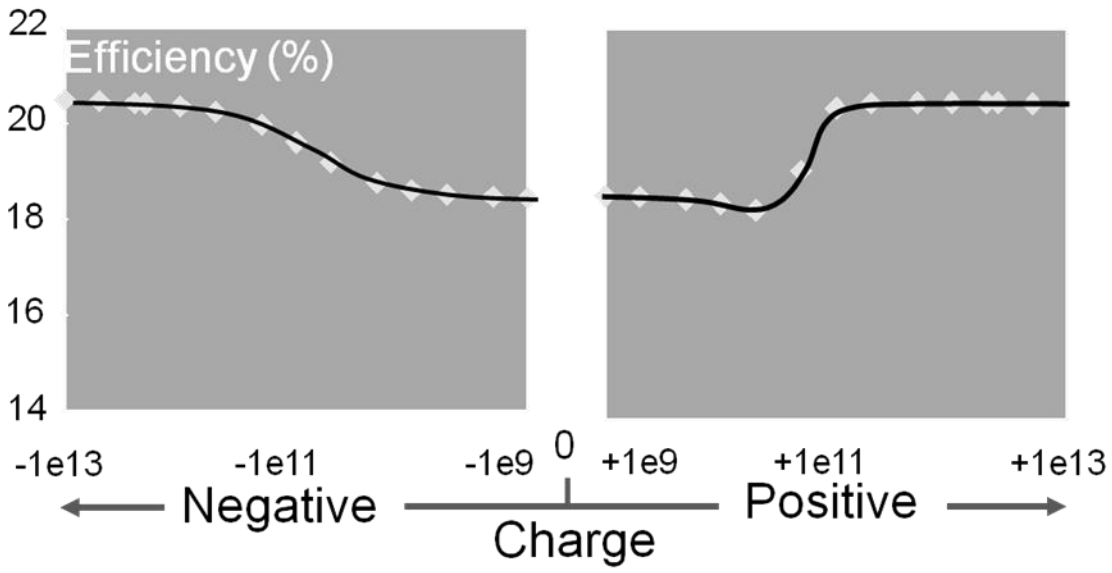


Figure 2.18: Results of 2D simulations showing dielectric charge required for high efficiency LBSF solar cells

One such dielectric that is being increasingly used in the novel cell structures is Al_2O_3. There are several methods of depositing Al_2O_3 and has been found to have a high negative charge exceeding 1×10^{12} cm^{-2}[41], which based on the earlier simulations, indicates the potential for cell efficiencies >20%. This has been demonstrated on PERC type cell structures with reported efficiencies of 20.6% when using a deposited Al_2O_3 (30 nm) with a PECVD SiO_x cap along with an evaporated Al for rear contact and reflector. This cell structure can be seen in figure 2.19 [42]. As with other high efficiency PERC type cells, this combination results in a BSRV of ~70 cm/s and a BSR of ~91%. A simpler device without the PECVD SiO_x but a thicker Al_2O_3 layer (130 nm) has also been reported with a peak efficiency of 20%. The lower efficiency is a result of a slightly higher BSRV of ~90 cm/s. These devices demonstrate the feasibility and potential of using Al_2O_3 as a passivating dielectric for the rear surface, but involve the use of

photolithography for definition of front and rear metallization and hence would need substantial modification to be adapted for large scale industrial manufacture.

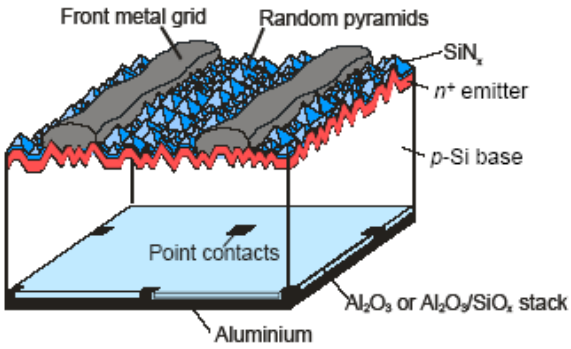


Figure 2.19: Schematic of Al_2O_3 rear passivated cell [42]

Another class of dielectrics that have been shown to produce high cell efficiencies is amorphous silicon. Cell efficiencies over 21% have been demonstrated with these dielectrics [43, 44]. The advantage of amorphous silicon is that it can passivate the surface better than a thermal oxide or Al_2O_3 resulting in cells BSRV of <50 cm/s and V_{OC} exceeding 670 mV. A schematic of the resulting cell is included as figure 2.20. The type and charge of a-Si can also be controlled during deposition making it a very flexible dielectric for different cell structures. However the one big drawback of using a-Si is its lack of stability of passivation at temperatures higher than 300 °C. As a result this dielectric is not suitable for screen printed contacts which undergo firing at higher temperatures. The use of photolithography for contact definition would render this technology complex and expensive for large scale industrial production.

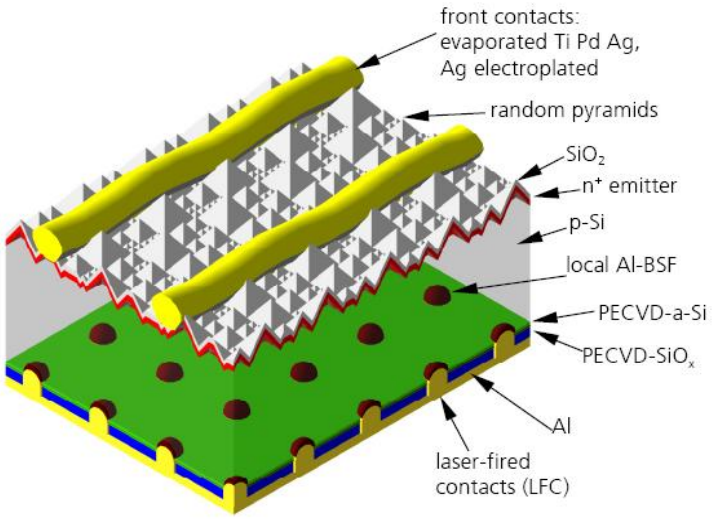


Figure 2.20: Schematic of a-Si rear passivated cell structure

2.5 Limited Source Diffusion using Dopant Solutions

The standard process employed in the industry for the formation of emitters is tube diffusion using $POCl_3$ as the phosphorous source. This process is convenient and feasible for the simple diffusion required by full Al BSF cell designs. However as we move towards the newer cell designs, there is a requirement for phosphorous diffusion only on the emitter leaving the rear surface undoped or doped with Boron. Currently, the diffusion is etched off the rear surface after diffusion. Studies are ongoing for alternate means of obtaining single sided diffusion like implantation [45] and inline diffusion [46]. Implantation provides the flexibility in terms of single side diffusion, type of dopant and would also be an easier method of obtaining selective emitters or any modified emitter designs. Another advantage of the implantation process is that it is already used extensively in the integrated circuit (IC) industry and can be meshed seamlessly with the

PV industry. However, the cost and energy requirements of the implantation process are substantially different from conventional tube diffusion and this necessitates further studies before being embraced by the PV industry. Inline diffusion employs spin-on sources for diffusion. Studies using inline diffusion have shown cell performance quite comparable to conventional diffusion methods [47]. In this work, a spin-on source in a conventional diffusion tube to obtain an emitter while another spin-on dielectric is simultaneously employed for rear passivation and keeping the rear surface free of diffusion. This method of using limited sources for dopant diffusion has been studied previously for use in the IC and the PV industries. The factors affecting these processes and some of these results will be discussed in the following section.

Limited source diffusions were originally performed by using Phosphorous and Boron source wafers. In this process, the wafers to be diffused, referred to as target wafers, were stacked alternately with the source wafers leading to the deposition of the dopants on the target wafer, forming a glass. This is followed by a drive-in step in a suitably designed process sequence. Sheet resistance and profile designs are modified by the concentration of the dopant in the source and process time and temperatures. This process was studied originally for adoption in the IC industry for diffusion of Boron and Phosphrous [48]. One advantage of this process is that, it removes the need to handle the highly toxic dopant bubblers.

2.5.1 Development of a Spray-on Dopant Process at Georgia Tech

A modification of this process is the use of spin-on or spray-on dopants as a diffusion source. There are several commercially available diffusion sources and the procedure for using these is fairly simple. These sources are designed for use directly on the cell wafers. These sources are spun-on or sprayed-on the wafer and then the wafers are dried either directly on a hotplate or in an oven. At this stage the low temperature solvents are dried out of the solution and wafers are ready to load into a tube or onto a belt. The high temperature process in the tube or belt furnace, as with the solid sources, leads to formation of the dopant glass and drive-in of the dopants. Both of these processes have been shown to result in cell efficiencies that are comparable to cells with conventional $POCl_3$ emitters [49, 50].

2.5.2 Diffusion using Spin-on Dopant Solutions

The choice of spin-on-solutions-based technologies has its positives and negatives. Solution-based processes can afford the advantages of cost, throughput, and ease of incorporation into modified cell structures. However, emitters formed using solutions in general are less uniform over a wafer than are conventional tube diffusions that use $POCl_3$ as a phosphorous source [51]. This uniformity is known to be further affected by environmental factors such as temperature and humidity [52]. General inhomogeneities, variations in sheet resistance, and surface concentration are the common non-uniformities observed in such diffusions that can adversely affect the quality of cells made on wafers with a large area [53]. There are several processing parameters that influence the quality of the diffusion, an effective understanding of which may be used to improve the

diffusion uniformity and cell performance, while retaining the flexibility of being incorporated into novel cell processes.

One such technology was studied in detail at Georgia Tech leading to the cell efficiencies over 20% and is considered a precursor to this work. In that work, conventionally available P and B sources were used to simultaneously diffuse the emitter and the BSF on cells. The limited sources were created by spinning-on the source solutions on "source" wafers which were loaded in the slots adjacent to target wafers in a quartz boat of a conventional tube furnace. On drying the following reactions occur resulting in the P and B sources forming on the source wafers as P_2O_5 and B_2O_3.

$$4\ POCl_3 + 4\ O_2 + Si \leftrightarrow 2\ P_2O_5 + SiO_2 + 6\ Cl_2 \quad (2.27)$$

$$4\ BBr_3 + O_2 + Si \leftrightarrow 2\ B_2O_3 + SiO_2 + 6\ Br_2 \quad (2.28)$$

The process was also designed to include an in-situ oxidation step producing a thick thermal oxide (1000 Å) as an anti-reflection coefficient on the textured surface. As a result, the target wafers were diffused and passivated in a single high temperature step and after definition of contacts using a photolithography (PL) process were ready for testing. These STAR cells had a peak efficiency of 20. %. A simpler cell design called STAR II with a thinner thermal oxide (100 Å) and a PECVD SiO_2 rear passivation was also developed, which resulted in a peak efficiency of 20.3%.

These cells combined the advantages of a PERC type cell with that of spin-on diffusion. One of the main factors in using this process with spin-on sources was that the PSG and

BSG remaining on the surface of the target wafers was found to be very thin (30-40 Å) which removed the need for glass removal after diffusion and resulted in a more streamlined process flow. It was concluded that another advantage of using this process for diffusion of B was that the impurities in the B source were left behind in the BSG on the source wafer and only the dopants migrated to the target wafer, hence maintaining the high lifetime necessary to fabricate high efficiency solar cells [54]. A schematic of the loading sequence used in the fabrication of the above cells can be seen in figure 2.21 and the resultant cell performance can be seen in table 2.1**.** This provides a good starting point for the development of this technology further to fabricate high efficiency solar cells with the potential for application in large-scale industrial production.

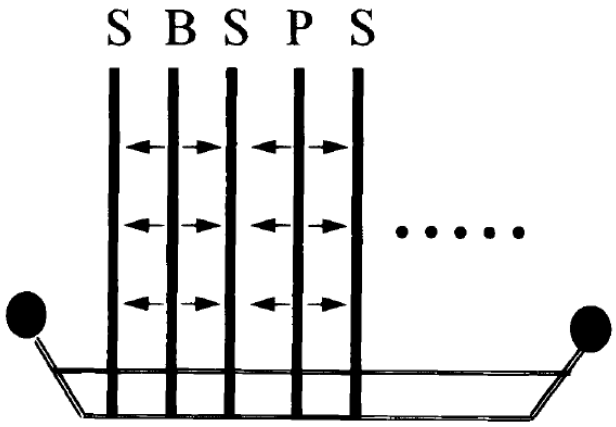


Figure 2.21: Wafer stacking arrangement in furnace boat for simultaneous boron and phosphorus diffusion. The front sides of the solar cells (S) are facing phosphorus oxide sources (P), while the back sides are facing boron oxide (B) sources

Table 2.1: IV data of the best STAR type cells [28]

	STAR	STAR II
Resistivity	2.0	2.3
VOC (mV)	643	645
JSC (mA/cm^2)	39.3	39.9
FF	0.796	0.788
Efficiency (%)	20.1	20.3

2.5.2.1 Challenges of using Spin-on Dopant Process for Diffusion

While this work outlined a good technology solution for the fabrication of high efficiency cells, this also identified that targets that must be achieved and a few issues that must be resolved before adapting this process on a larger scale. One of the major problems involving the spin-on source was the shelf-life of the source and its sensitivity to ambient conditions. Firstly, this source would have to be refrigerated to maintain consistent performance over regular use and this would add a level of complexity to the processing. Secondly, it was noted that the resulting sheet resistant was very closely related to the ambient humidity as this affected the quality of the source-film and hence subsequent diffusion. These are both seen as inherent problems associated with commercial sources and would need to be addressed in the future. In addition to these process-related deficiencies, these high efficiency cells were fabricated with the use of PL for defining contacts. As with the PERL technology, this renders the process expensive and lengthy

and would need to be modified to include screen printed contacts for compatibility with industry standards. However, the passivation schemes used in these devices might not continue to be effective when subjected to the firing process and would hence need to be modified accordingly.

This suggests that while this work presents a good template for future work, sufficient modifications would need to be made with the passivation schemes and contacting methods. Addressing the uniformity and stability issues of spin-on solutions are also important for the future of this cell design. In addition, the advantages of not using Boron as a full BSF need to be investigated to employ a more robust and less complicated cell structure. Towards these goals, two other results obtained at Georgia Tech are of particular importance. The first was the development and use of in-house spin-on solutions which address the primary concerns of stability and lifetime of the phosphorous source. The second work involved the development, through modeling and fabrication, of a local back surface field design that displays the potential of high efficiency cells.

2.5.2.2. Development of Non-commercial Phosphoric Acid Sources

The first work laid the foundations for the use of phosphoric acid for the development of in-house dopant sources [55]. A simple and repeatable method of using a high purity commercial phosphoric acid (85% H_3PO_4 in water) mixed with calculated quantities of DI water was used to make up phosphorous sources of different concentrations by weight. The concentration of phosphoric acid was represented by the equivalent weight percent of P_2O_5 in solution, which was calculated using the following equation

Equivalent percentage of P_2O_5 = (weight of P_2O_5)/(weight of H_3PO_4 + weight of water)

= 0.725 × (weight of H_3PO_4)/(weight of H_3PO_4 + weight of water). (2.29)

These sources were sprayed on wafers by a set-up specially developed for this study before diffusion using the standard inline method. The reaction involving phosphoric acid and silicon leading to emitter diffusion can be seen below.

$$H_3PO_4 + H_2O \rightarrow H_3PO_4 \rightarrow P_2O_5 \text{ (dehydration process)} \quad (2.30)$$

$$2\ P_2O_5 + 5\ Si \rightarrow 5\ SiO_2 + 4P \text{ (diffusion process)} \quad (2.31)$$

The various spraying parameters affecting the quality and the uniformity of the diffused emitters were identified to be belt speed, flow rate of the carrier gas and concentration of phosphoric acid. After optimization cells fabricated using this method were found to have only slightly lower efficiency (~0.3% absolute) compared to conventional $POCl_3$ diffused cells.

Based on these experiments some critical observations were made regarding the use of these in-house developed solutions. It was found that for good spreading and adhesion of the source, a hydrophilic silicon surface would be preferred. A hydrophobic surface was found lead to a non-uniform spreading and emitter. The hydrophilic surfaces can be obtained by simple chemical oxidation for a short duration (~5 minutes) in freshly prepared HCl or H_2SO_4 solutions before spray coating of the source. Another important

factor to be noted when using these solutions is that high concentrations of this source cause the precipitation of SiP on the Si surface, which adversely affects the quality of the emitter. The use of lower concentrations such as 2% P_2O_5 were found to result in high efficiency cells identifying these low concentrations as safe for use in future high efficiency cell structures. This work demonstrated the feasibility of using in-house spin-on sources while outlining the limitations and advantages of this technique. With the added flexibility of preparing any concentration that the process required, these solutions were expected to relatively free of the sensitivity to atmospheric conditions during storage and use, thereby eliminating some of the main problems associated with commercial spin-on sources. This was considered an important step for developing a high efficiency cell structure using spin-on solutions.

2.6. Development of Spin-On Based Rear-passivated Cell Design

Another critical step involved in the development of a high efficiency cell structure is the optimization of a rear passivation scheme that not only has an ideal charge but also ease of use and more importantly compatibility with a screen-printed contact process. The fundamentals of such a scheme were studied at Georgia Tech. Through a combination of modeling and characterization, a spin-on dielectric and PECVD SiN_X stack was identified as an ideal candidate. This dielectric stack was found to have a high positive charge of 1 - 3×10^{11} cm^{-3} and a recombination velocity that is comparable to a good thermal oxide (<35 cm/s). A suitable cell structure was conceptualized using a fully screen printed process, by employing a screen printable paste that would etch this specific dielectric stack, to define vias through the rear dielectric. A screen printing paste was specially

developed that would form a good quality LBSF through the vias, while maintaining the stability of the rear passivation after firing [56]. Also in combination with the dielectric stack, this rear structure was found to have a high back surface reflectance (BSR) of ~93%. All of these components combine all the benefits of good rear passivation in the high efficiency PERC type cells described earlier, indicating a potential for high efficiency. Initial experiments on planar wafers resulted in encouraging cell performance.

2.6.1. Challenges in Developing a High-efficiency Cell Structure

To achieve a truly high efficiency cell, this would have to be combined with a passivated high quality emitter, a textured front surface with screen printed front contacts. For the best results from this cell structure however, it was required that the rear surface be free of diffusion. Also to harness the high quality rear passivation by the dielectric stack, the rear surface would have to be planar. The process sequence for obtaining this through conventional methods would involve several extra steps to obtain not only the planar rear surface, but also diffusion only on the front surface. A simpler processing sequence would need to be designed that helped reach all these targets simultaneously. This work, in subsequent sections, describes in detail how a spin-on process was designed to maximize the performance of this cell structure while developing the foundation of future cell technologies.

2.7. Applications for Laser in PV processing

As with any other technology at the cutting edge, cost and throughput are major concerns in the PV industry. Simple full BSF cell technologies had reached optimal efficiencies without a substantial use of lasers. As the technology focus shifts towards advanced cell designs, there is an increased need for a better resolution of cell features and the higher precision that goes with it. Lasers are a solution being explored at various stages of solar cell fabrication to provide these advantages while adding precision, selectivity, throughput and other benefits specific to the PV cell fabrication, which are expected to together help reduce the cost of cell production to bring it closer to grid parity. Various types of lasers have been studied and used for wafer isolation [57], doping [58], contact firing [59] and selective ablation of dielectrics [60]. Laser structuring has been used for back junction solar cells and drilling holes through Si for EWT/MWT structures [61, 62] Lasers are also ideal solutions for doping of selective emitters using spin-on dopants [63], PSG [64] or another external doping source as in the case of LCP [65]. The particular demands of solar processing and the applicable properties of lasers for each function is detailed in table 2.2 below.

Table 2.2: Comparison of the demands of crystalline silicon solar cell production with the characteristic properties of laser radiation [66]

Demands of solar cell processing	Laser characteristics
Possibility to process different materials like silicon, dielectric layers and metals	By choosing the proper wavelength, absorption is sufficient for all materials
Single-sided processing	Low optical penetration depth and heat influence in crystalline silicon when using pulsed lasers (<1 μs) with short wavelengths (< 1 μm)
Generation of local structures	Most laser systems are capable to be focussed down to the necessary structure widths of 10-100 μm
Low / no mechanical influence on the substrates	Due to the contact-less nature of light possibility to use low-impact in-line production technology
High throughput at processing equipment (~ 2s / cell)	Applicability of scanning systems, beam splitting optics and additional laser sources in one machine

The use of lasers in solar cell manufacture is an important step towards better cell designs. It can be used as a simpler alternative for photolithography based processes, thereby reducing cost and complexity of processing for novel cell structures. In this study, lasers are used for selective ablation of rear dielectric to achieve a high efficiency cell structure. Prior to the use of lasers, these tasks were typically accomplished by the use of wet chemical etching and photolithography, or a plasma process. Long processing times typical of these processes render them infeasible for use large scale production. Selectivity of the laser is a particularly important need when ablating the dielectric from diffused surfaces or on surface whose passivation is important [67]. In these cases, the type of laser, the energy used and its effect on the silicon surface and bulk – optimal heat

affected zone - are critical to the final performance of the cell. The incident wavelength from the laser and its absorption in the silicon, as seen in figure 2.22, are critical to the appropriate choice of laser used for ablation. In this study, the dielectric removal is performed on an undiffused surface and does not introduce a new interface. However the quality of the via is considered a vital component for the formation of good contact and a uniform BSF, which ultimately is expected to reduce the effects of parasitic shunting surrounding the rear contact points.

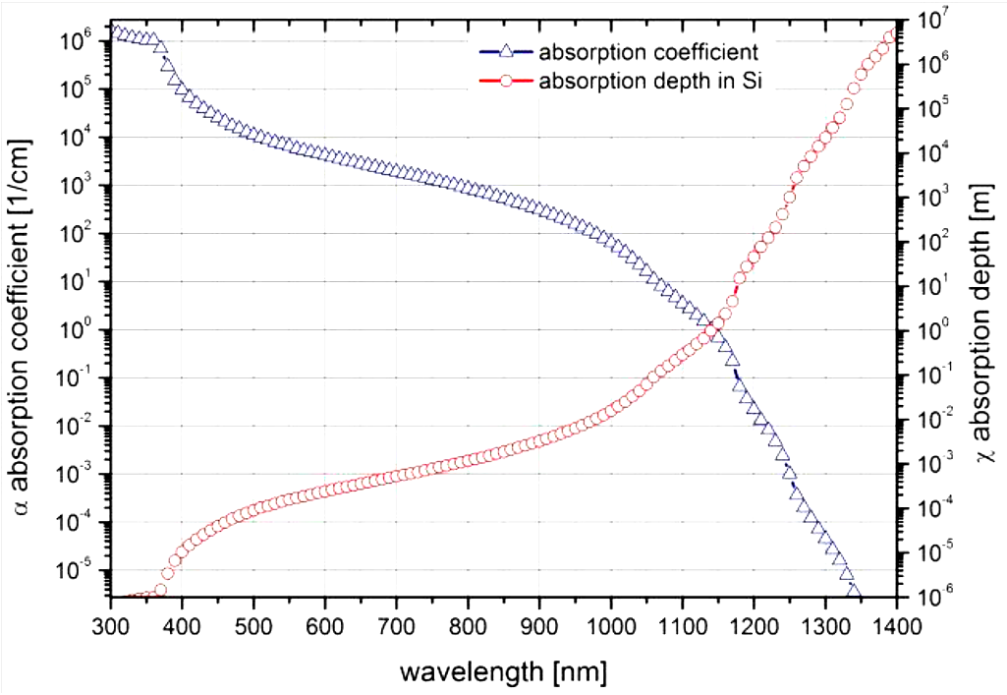


Figure 2.22: Optical properties of silicon: absorption coefficient (triangles) and absorption depth (circles) as a function of wavelength

The use of laser for selective ablation of dielectrics has been studied for various dielectrics such as a-Si:H [68], SiN_X, and SiO/ SiN_X stacks. UV and Green lasers have been identified as ideal choices for ablation of front and rear SiNx while limiting the

damage to the silicon surface and any emitter underneath [69, 70]. These wavelengths are found to be absorbed well in the SiNx layers and hence, when the energy per pulse is optimized, minimized the interaction with the silicon surface below the dielectric, as seen in figure 2.23. In addition, their limited penetration depths in solid and liquid Si ensure that very little energy is transferred to the silicon even after the complete ablation of the dielectric. Pulsed lasers with nanosecond pulsewidths have been used with the most success for these applications.

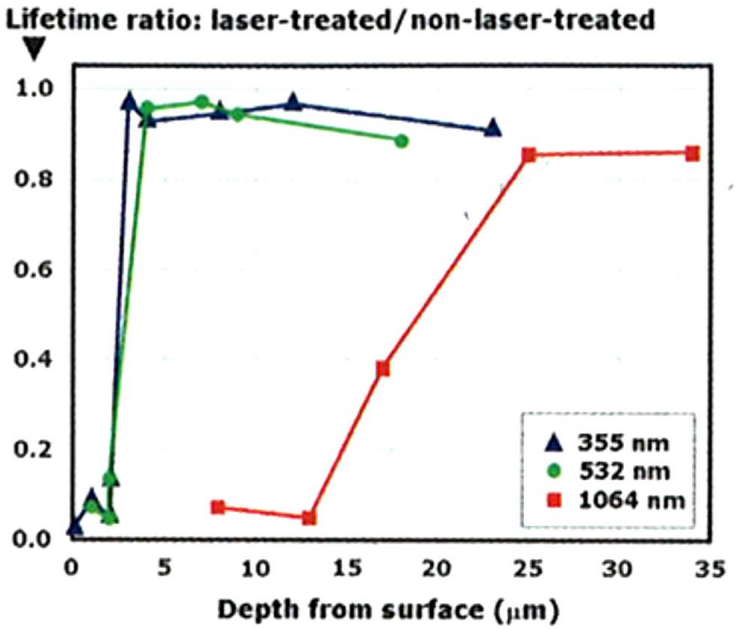


Figure 2.23: Comparison of the effect of ablation on SiNx passivation by three different lasers on wafer lifetime

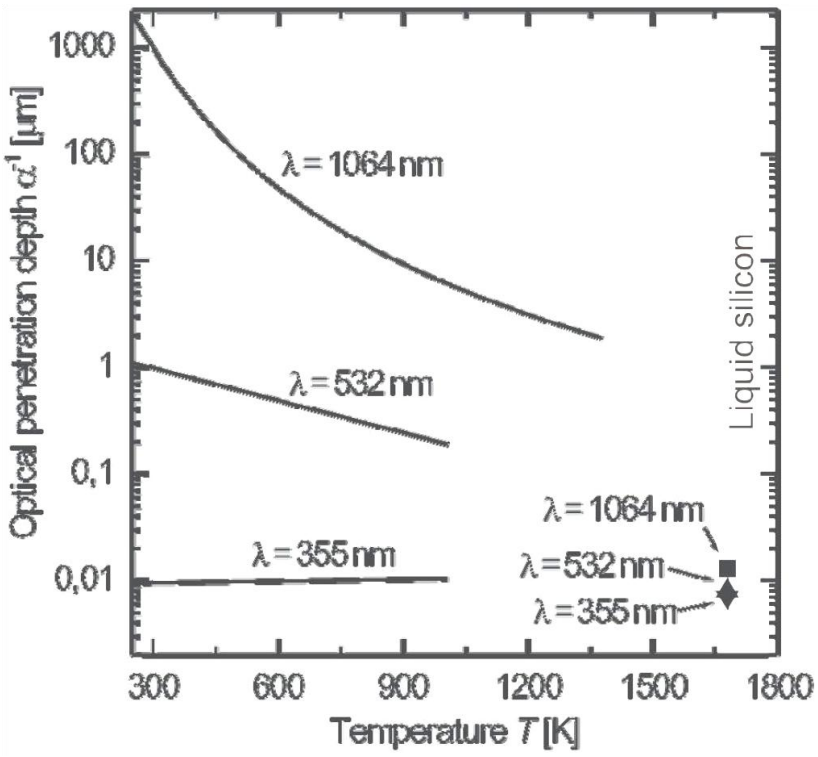


Figure 2.24: Dependence of laser penetration in Si as a function of material temperature

Ablation of SiO_2 layers is considered a bigger challenge for lasers. Laser wavelengths need to be much than 300 nm to be absorbed by SiO_2 and hence, the typical method of ablation of oxides is to melt the silicon surface below and cause a removal of the oxide in the resulting expansion. Ablation of the SiO_2 rear dielectric by a 286 nm KrF excimer laser has resulted in the fabrication of high efficiency RP-PERC cells [71]. Another study for removal of front passivating SiO_2 for use in selective emitter structures revealed that lasers with very short pulsewidths (nanosecond or lower) are more preferable for limiting damage to the emitter below [72].

In this thesis, a comparative study of various lasers for ablation of a dielectric stack is presented. Since the dielectric stack consists of a PECVD SINx and a spin-on glass, the

use of laser needs to be carefully optimized to remove all of the nitride and then melt enough of the silicon surface to remove the thick spin-on oxide. The use of lasers, in this particular study, is expected to improve uniformity over the entire wafer surface and from wafer to wafer in a batch. It is expected that laser ablation will make this technology relatively independent of the wafer surface, wafer thickness and rear dielectric stack employed making it suitable for use in large scale production over a wider range of technologies and cell designs.

2.8 Conclusion

In this chapter, an overview of various components that can combine to improve cell efficiency has been provided. Some of these are utilized in this thesis and have resulted in a high efficiency cell structure that forms a template for future cell technologies. These technologies are capable of reducing the cost-per-watt metric of solar cells, thereby helping us attain grid parity. A detailed look at how these components were combined will be provided in subsequent sections.

CHAPTER 3

DIFFUSION USING SPIN-ON SOLUTIONS

3.1 Introduction

Spin-on solutions based processes are being investigated for low-cost front- and rear-junction formation and passivation for next generation solar cells. Recently published results show good improvement in solar cell efficiencies with the use of such solutions [73]. Solution-based processes offer the advantages of cost, throughput, and ease of incorporation into modified cell structures. However, emitters formed on textured surfaces using solutions are often less uniform over the entire wafer relative to conventional tube diffusions with $POCl_3$ source.

There are several processing parameters that influence the quality of the diffusion. Improved understanding of process control can improve the diffusion uniformity and cell performance. Therefore, in this study, a limited source diffusion process was developed that uses a phosphoric acid dopant source applied on a source wafer that is loaded adjacent to the sample wafer in a quartz boat. This work shows that optimization of the diffusion process and gas flow can produce high quality emitters with good uniformity which is not affected by ambient conditions. The optimized process was then applied to improve the emitter uniformity of a spin-on process that produced high cell efficiency on full BSF cells.

3.2 Development of a spin-on-solution-based diffusion process

This work involves the development of a spin-on diffusion process for emitter formation. The diffusion source was prepared in-house using phosphoric acid and diluted with DI water and ethanol. This source was then used with a limited source diffusion process involving a stacked source and target wafer arrangement described in the earlier chapter, to obtain an emitter on silicon wafers for cell fabrication. There are several advantages of using this method for diffusion. Firstly, a high quality emitter can be obtained without a thick phosphorous rich glass on the target wafer. This removes the need for an additional glass removal step during processing. In addition, advanced cell structures can make use of in-situ oxidation to grow a passivating oxide on the emitter with a simplified furnace process. Secondly, the use of a simple non-commercial phosphoric acid source increases the flexibility in tailoring emitters and diffusion processes to suit the application while reducing sensitivity to room temperature and humidity. This phosphoric acid source also has higher shelf life compared to commercial sources and does not need refrigeration, thereby, resulting in easier and more reliable processing.

The process sequence involved cleaning the source and target wafers before diffusion. The source wafers were then subjected to an additional step to grow a chemical oxide on the surface. This helps the adhesion of the phosphoric acid to the wafer. The phosphoric acid solution of the required concentration was made up by diluting the stock solution with calculated amounts of high purity ethanol. Ethanol was used as a solvent to promote uniform spreading of the acid solution over the entire source wafer. The solution was

then spun-on the source wafer using an optimized spinning condition. Source and target wafers were then loaded into the diffusion furnace, stacking the source and target wafers alternately while keeping the dopant side of the source wafer facing the front or emitter side of the target wafer, as seen in figure 3.1.

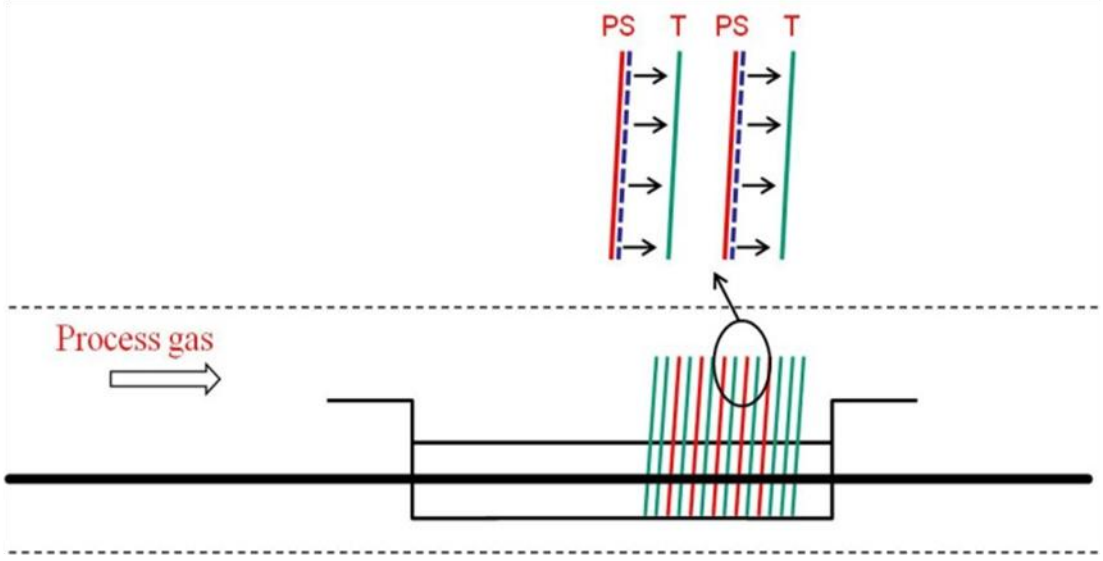


Figure 3.1: Stacking diagram showing the configuration of source and target wafers

3.1.1 Understanding the Factors that control Limited Source Diffusion

There are several factors that needed optimization to obtain a high quality emitter suitable for high-efficiency cells. The following four factors were identified and optimized in this research:

1. Diffusion temperature
2. Time at high temperature
3. Phosphoric acid concentration
4. Gas flow during processing

The relationship between these parameters was found to be important to engineer a dopant profile that is ideal for a screen-printed contact. The first three parameters were optimized with a basic understanding of diffusion processes, while the fourth factor was specific to the diffusion process used in this research. Screen printed cells require surface concentration of $>5 \times 10^{19}$ cm^{-3} to ensure a low specific contact resistance under the front contact metal grid [74], which is important for achieving high fill factor and high-efficiency screen printed cells. The surface concentration of phosphorous is also critical for passivation of the emitter, which affects the V_{OC} of the cell. Since lower surface concentration tends to give better surface passivation, there is a need to optimize it so that it would give low contact resistance and a low FSRV simultaneously.

The relation between diffusion temperature and time for a limited source is identical to a conventional $POCl_3$ process – high process temperature leads to lower sheet resistances and longer process times lead to deeper emitter profiles. The concentration of the phosphoric acid source adds the flexibility of varying the amount of available phosphorous in the limited source, making it easier to control the sheet resistance, surface concentration and the emitter profile. The fourth factor was more specific to this limited source diffusion process and involved understanding the transfer of dopants from the source to the target wafer.

3.2 Experimental Setup for Studying the Effect of Gas Flow on Diffusion

In this study, diffusion uniformity was analyzed by mapping sheet resistance over the area of each wafer. All emitters and solar cells analyzed in this study were fabricated on 300 μm thick 100 mm FZ wafers. Diffusion, followed by in-situ oxidation was performed on these wafers using the STAR process referred to in Chapter 2 [53]. Planar FZ wafers were used as source wafers. These wafers are loaded in a quartz boat with a wafer-to-wafer spacing of 0.24 mm. Diffusion processes were performed in a N_2 or inert gas ambient with N_2 flow rates of 1 lpm, 3 lpm, and 5 lpm during ramp-up and steady-state diffusion. In one case, the gas flow was varied between the ramp-up and steady-state steps to understand its effect on diffusion uniformity. It is important to note that the source wafers are reused for subsequent diffusions. Some wafers were also diffused in a tube furnace using conventional $POCl_3$ technology to serve as a reference to compare diffusion uniformity of $POCl_3$ and STAR technologies. Sheet resistance measurements were made on 49 points over each wafer and analyzed. Results of these experiments can be seen in figure 3.2.

3.3 Discussion of the Effect of Gas Flow on STAR Diffusion Process

Sheet resistance measurements indicated a significant impact of gas flow on the uniformity of diffusion over the entire wafer. Gas flows of 1 lpm and 5 lpm resulted in non-uniform sheet resistance over a 100 mm wafer. In these cases, sheet resistance was found to be low at the center and increased gradually towards the edges. Diffusion profiles on these wafers indicated a high surface concentration of phosphorous at the

center and a lower concentration on the outer fringes. Since surface concentration is a critical factor in determining contact quality, this non-uniformity can result in lower fill factor and lower efficiency for screen printed solar cells compared to a $POCl_3$ emitter cell[75]. Based on prior studies on gas flow dynamics of such processes [76], it is proposed that 1 lpm is too low a rate to cause a steady and uniform transfer of dopants from source to target wafer. On the other hand 5 lpm is too high, which could cause in turbulence between the source and target wafers and result in severe non-uniformity in sheet resistance. It was found that diffusion uniformity improved significantly with the gas flow of 3 lpm compared to 1 lpm and 5 lpm. Standard deviation of measured sheet resistance in this case decreased from ~14 ohm/sq to ~4 ohm/sq. While this non-uniformity can still manifest itself as low fill factor, the standard deviation compares favorably with that of standard $POCl_3$ diffused emitters. Thus, gas flow rate is critical for spin-on solution-based diffusion process and for our experimental specifications, 3 lpm was found to be optimal.

A second study was conducted to see the impact of changing gas flow between ramp-up and steady-state steps. 3 lpm during ramp-up and 1 lpm during drive-in provided a good insight into the mechanism of this diffusion process. The spread in sheet resistance on the wafer indicated that increasing the nitrogen flow from 1 lpm to 3 lpm during ramp-up improved the emitter uniformity. Thus, 3 lpm seems to be the optimal flow rate for this diffusion for both the steps. These results indicate that dopant transfer occurs between the source and target wafers during ramp-up as well as during the steady-state diffusion. The positive effect of higher gas flow during ramp-up also indicates that the majority of this

transfer happens during ramp-up and that the steady-state step at process temperature serves to drive-in the P deposited on the surface of the target wafers during the earlier ramp-up step. It was also observed during these tests that both the average sheet resistance and uniformity of diffusion were affected by ambient humidity.

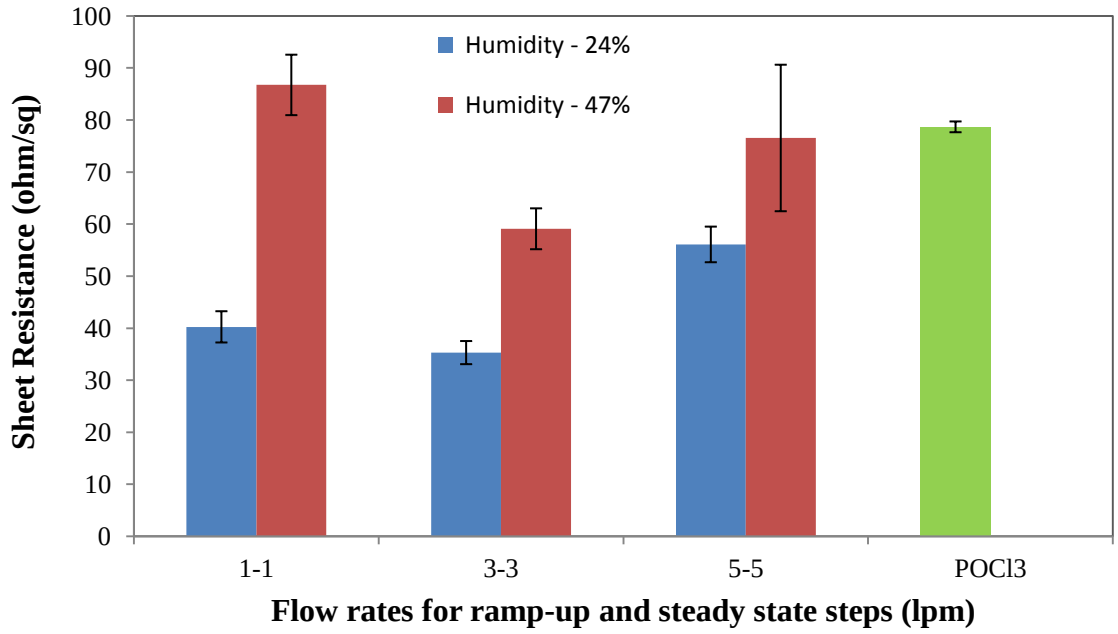


Figure 3.2: Measured sheet resistance values for a $POCl_3$ diffused wafer and the STAR diffused wafers with three different gas flow rates (lpm) during ramp-up and steady state

3.4 Development of Modified STAR Process for Diffusing Improved Emitters

This understanding was then applied to develop a diffusion recipe for cells that can lead to lower emitter saturation current density (J_{oe}) [77]. It was also found that if the wafers are subjected to a short oxidation step immediately after loading at 700 ºC, it enables the formation of a diffusion glass on the source wafer and results in a lower J_{oe}. Subsequent ramp-up and drive-in resulted in a more controlled transfer of dopants from source to target wafer. This results in improved uniformity and J_{oe}. To confirm this, planar and textured wafers were diffused on both sides using 4 different processes shown and their respective J_{oe} were measured as seen in figure 3.3. The lowest J_{oe} resulted on wafers subjected to the "pre-oxidation" process prior to diffusion. On textured wafers the best J_{oe} obtained was ~100 fA/cm^2 and planar wafers had a J_{oe} of ~80 fA/cm^2. Combined effect of the increased surface area of textured wafers and the use of limited source, resulted in lesser dopants per unit area on the textured surface than the planar surface, which resulted in a slightly higher sheet resistance on textured wafers compared to planar wafers for the identical diffusion conditions. Emitters obtained through this process also had high surface concentration of P (~1E20 cm^{-3}) with very little variation in profile between center and the outside of each wafer, which is important for screen printed contacts. The improvement in the emitter Joe due to the pre-oxidation process should contribute to an increase in cell V_{OC}, J_{SC}, and cell efficiency.

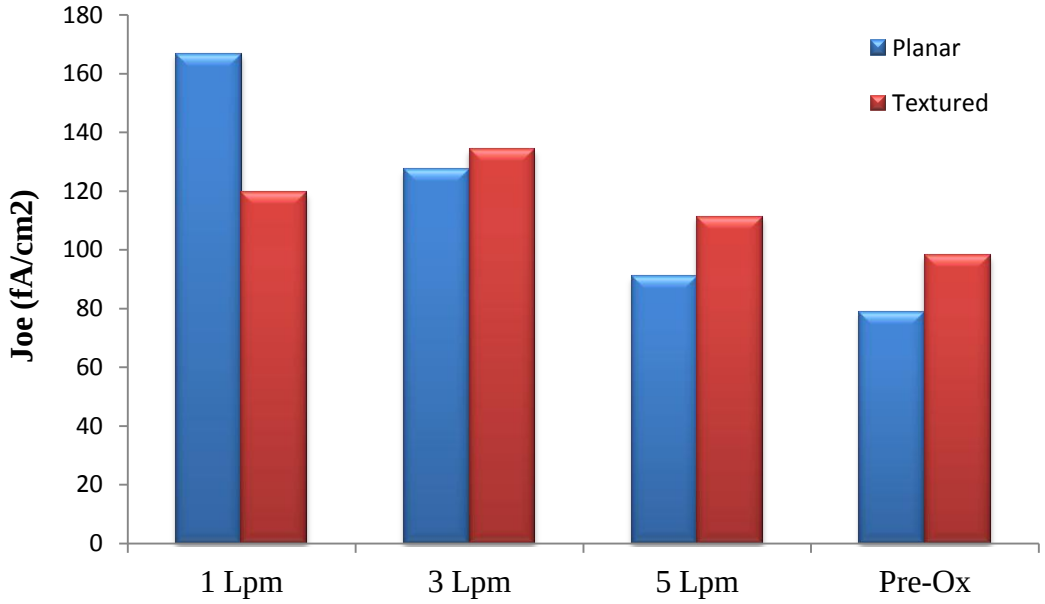


Figure 3.3: Measured Joe as a function of diffusion process parameters

The above diffusion parameters were optimized to obtain a high sheet resistance (~75 Ω/□) emitter for high efficiency cells. The optimized emitter profile is shown in Figure 3.4 with an emitter depth of 0.65 um with surface concentration of 9×10^{19} cm^{-3}. The higher surface concentration is good for screen printed contacts and the shallower junction depth helps reduce recombination within the emitter, thereby lowering J_{oe}. Note that the surface concentration is comparable to commonly obtained high sheet resistance emitters using the standard $POCl_3$ process. The performance of this emitter was tested with respect to $POCl_3$ diffused emitter using a standard screen-printed full BSF cell structure. Prior studies have revealed the benefits of using a high sheet resistance emitter with a full BSF on low resistivity substrates [78].

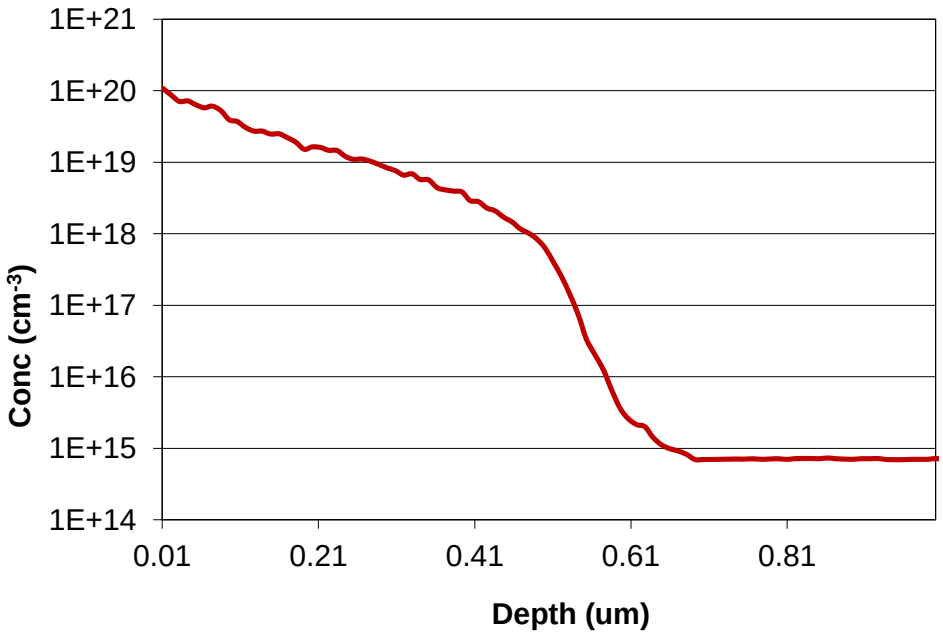


Figure 3.4: Optimized phosphorous profile for high sheet resistance emitter

3.4.1 Effect of Humidity on Modified STAR Diffusion Process

Prior work at Georgia Tech, on the STAR diffusion was performed using commercial spin-on sources [51]. While it resulted in high efficiency cells (> 20%), ambient humidity was found to adversely affect process reliability [79]. Sheet resistances obtained from commercial sources were found to be affected significantly by ambient humidity as seen in figure 3.5. This variability adversely affected the reproducibility of high efficiency cells. However, sheet resistance data obtained from using in-house prepared phosphoric acid solution in conjunction with this "pre-oxidation" process showed that the process results were less sensitive to ambient humidity. As seen in figure 3.6, fluctuation in humidity of ~28% produced a tighter distribution of average sheet resistance on a wafer compared to the previous results using a commercial source as seen in figure 3.5 [51]. It

should be noted that the targeted sheet resistance of 75 Ω/□ for high efficiency cells was within the accepted tolerance limits (± 5 Ω/□) for this process.

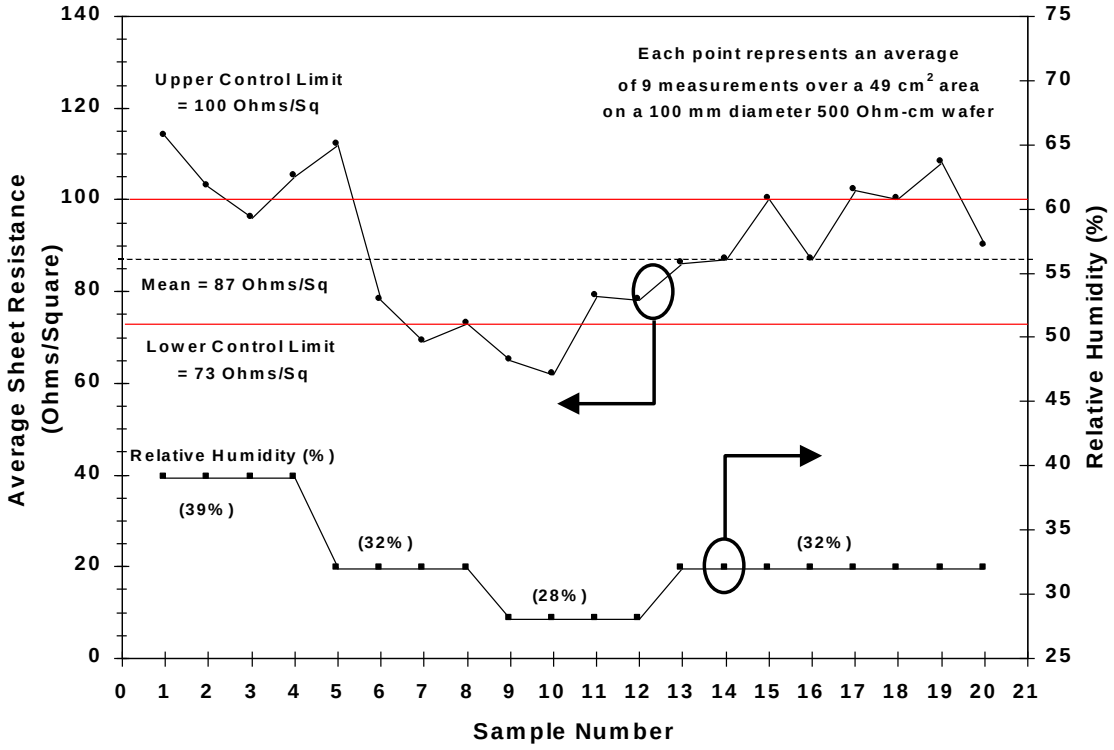


Figure 3.5: Effect of humidity on average sheet resistance with STAR process [51]

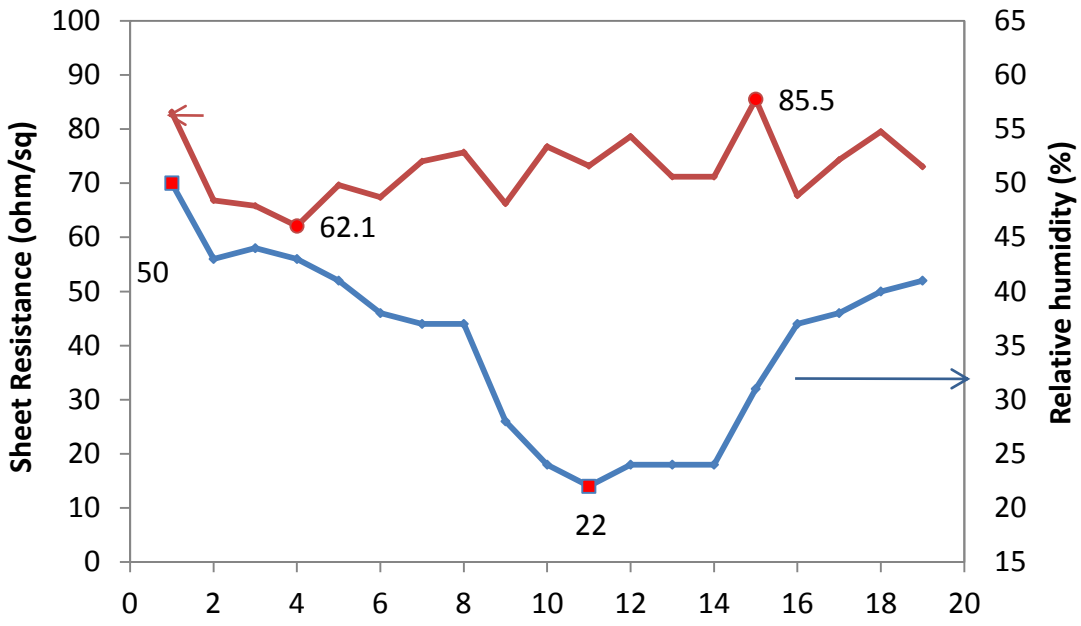


Figure 3.6: Distribution of average sheet resistances measured on batches processed with varying ambient humidity

3.5 Fabrication of High Efficiency Cells Using Limited Source Diffusion

Complete cells were fabricated on textured 300 µm thick float zone (FZ) wafers with a resistivity of 0.6 Ω.cm. Simulations performed in a previous study at Georgia Tech showed that low resistivity substrates produce higher efficiency on a full BSF cell structure. This resistivity choice also facilitates an easy comparison with prior work at Georgia tech using high sheet resistance emitters [79]. Cells, with emitters obtained with the aforementioned STAR process, were coated with a PECVD SiNx on the front for passivation and anti-reflection properties. Screen-printing was used to define aluminum (Al) contacts on the rear and a silver (Ag) grid on the front. Contact co-firing was

performed in a belt furnace. There were 9 cells on each wafer, each with an area of 4 cm^2. They were isolated electrically from each other using a process of cutting through the p-n junction using a dicing saw and a chemical etching of the groove formed by the dicing saw. Prior to dicing the cells using the dicing saw, the wafer surfaces were protected with a photoresist. This ensured that the chemical etching only occurs in the silicon exposed in the dicing grooves. These cells were tested following an anneal at 400 ºC in an atmosphere of forming gas. The complete process sequence is shown in figure 3.7

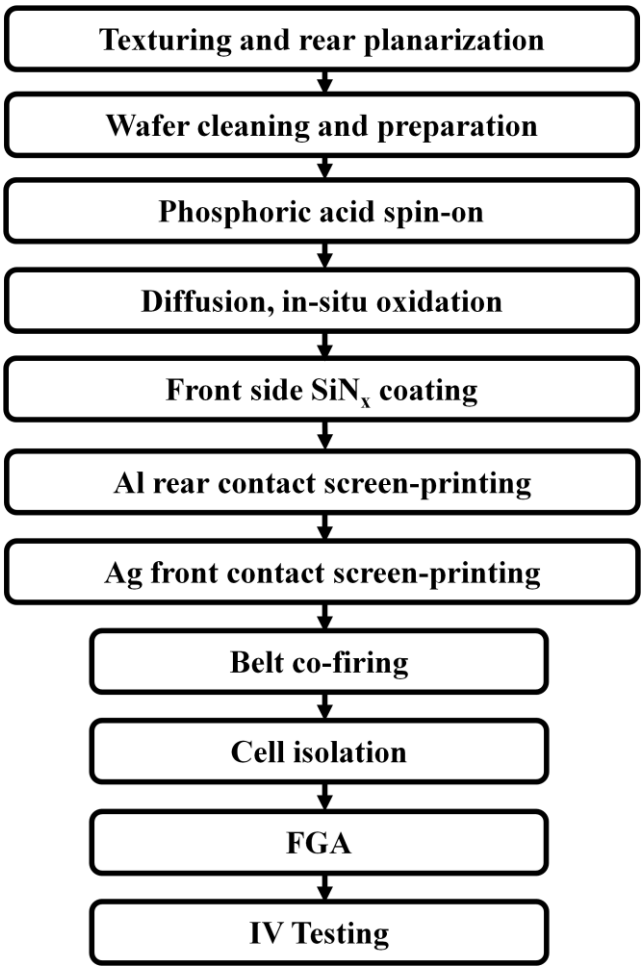


Figure 3.7: Schematic of process sequence used in fabrication of high efficiency full Al BSF solar cells

The best cell obtained using this emitter and a full BSF cell structure had an efficiency of 19.6% with a V_{OC} of 648 mV and a J_{SC} of 37.5 mA/cm^2 (Table 3.1). More than 50 cells were fabricated using this cell design and the process average with an average efficiency of 19.2%. This was superior to the best cell reported in the literature with a similar cell structure and size [79]. All cell results shown in table 3.1 were validated at NREL. A better front surface passivation due to the higher sheet resistance is the primary reason for the improved V_{OC} and efficiency compared to the literature. A low series resistance of 0.51 Ω.cm^2 was measured due to the optimal surface concentration and profile of a high sheet resistance emitter used in this study. This led to a high fill factor of 80.4 % leading to high cell efficiency. As a result of the optimization of the dopant transfer process with pre-oxidation process and proper gas flow rates, the uniformity of diffusion and cell performance was high, supported by several similar high efficiency cells on the same wafer, as seen in figure 3.8.

Table 3.1: Cell parameters measured using IV testing

Cell	V_{OC} (mV)	J_{SC} (mA/cm^2)	Efficiency (%)	FF (%)
Best Cell (Previous work)	643	37.8	19.0	78.1
Best Cell (Current work)	648	37.5	19.6	80.4

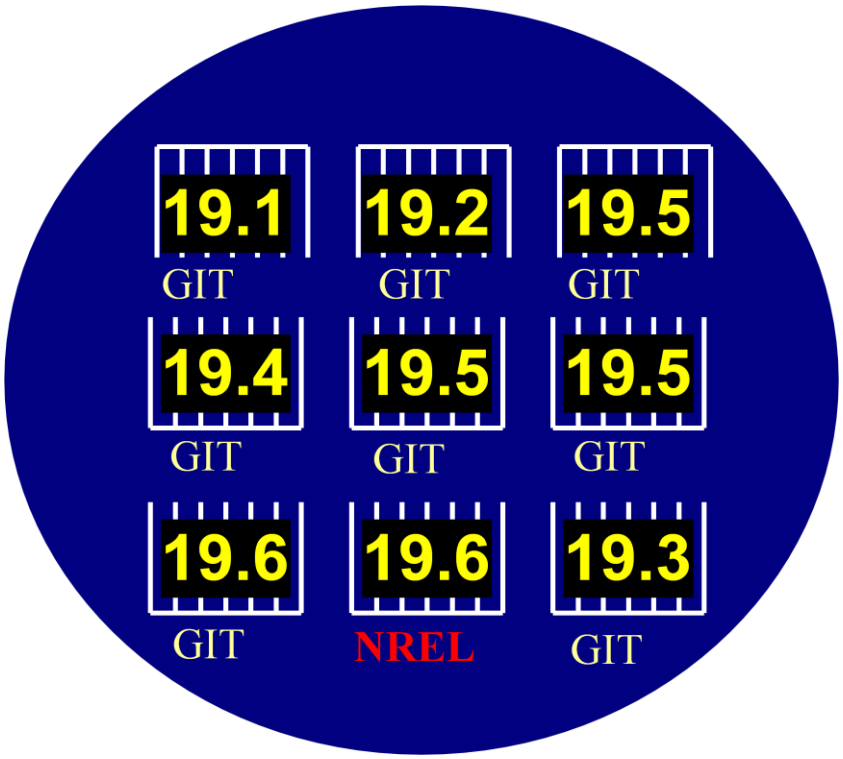


Figure 3.8: Distribution of cell efficiencies on high efficiency wafer

3.6 Characterization of Record High Efficiency Full Al BSF Cell

Further characterization of these cells was performed to complete the understanding of the factors that led to record high efficiency full Al BSF cells in this study. This was done with the help of I-V, Suns-V_{OC}, IQE and reflectance measurements. This data is summarized in Table 3.2 along with the data for the 19% cell from literature. Modeling revealed improvements in two regions, which contributed to a significant improvement in cell performance – the front passivation and improved edge isolation. The passivated emitter diffused using the limited source method developed in this research resulted in improved front surface passivation, in spite of having a lower sheet resistance compared

to the 19% cell in the literature. This is supported by much lower front surface recombination velocity (Table 3.2). The in-situ oxide in combination with the PECVD silicon nitride gave superior passivation when compared to the single layer silicon nitride on the literature cell. Table 3.2 shows that improved emitter and passivation resulted in an increase of 7 mV in V_{OC} relative to the 19% cell. Another notable improvement was in junction leakage current, J_{02}. The improvement in the J_{02} is attributed to the improved cell isolation process which involved a chemical etching step after isolating with a dicing saw. Thus, increased V_{OC}, reduced $J_{02,}$ low series resistance and high shunt resistance combined resulted in the high fill factor and a high cell efficiency.

Table 3.2: Summary of parameters used for PC1D modeling of Full Al BSF cells

Cell Parameters	Previous work	Current work
Base Resistivity (Ω.cm)	0.6	0.6
Rs ($\Omega.cm^2$)	0.79	0.51
Rshunt ($\Omega.cm^2$)	68157	46200
n2	2	2
J_{02} (nA/cm^2)	18	8.316
Emitter sheet resistance (Ω/sq)	100	75
Surface conc (cm^{-3})	1.50E+20	5E+19
Tau bulk (µs)	250	250
BSRV (cm/s)	600	600
BSR (%)	61.5	68
FSRV (cm/s)	60000	13000
Grid shading (%)	~4-4.5	~4-4.5
Modeled Voc (mV)	640	648
Modeled Jsc (mA/cm^2)	37.3	37.4
Modeled Eff (%)	19	19.5
Modeled FF (%)	79.6	80.4

Note that the best cell had a series resistance of 0.51 $\Omega.cm^2$ and a high fill factor of 80.4 %. To confirm that the emitter profile with high surface concentration contributed to a low contact resistance, some of these cells were characterized further using the transmission line method (TLM) [81]. The TLM pattern was screen printed and fired along with cells and then isolated from the rest of the wafer prior to measurements. Specific contact resistance between these screen printed contacts and the emitter was calculated to be 1.6 $m.\Omega.cm^2$. This data had an r-squared fit of 99.93% to the measured resistances as seen in figure 3.9. This specific contact resistance is very low and further proves that the optimized process using a phosphoric acid source is well suited for fabrication of high efficiency cells using screen printed contacts.

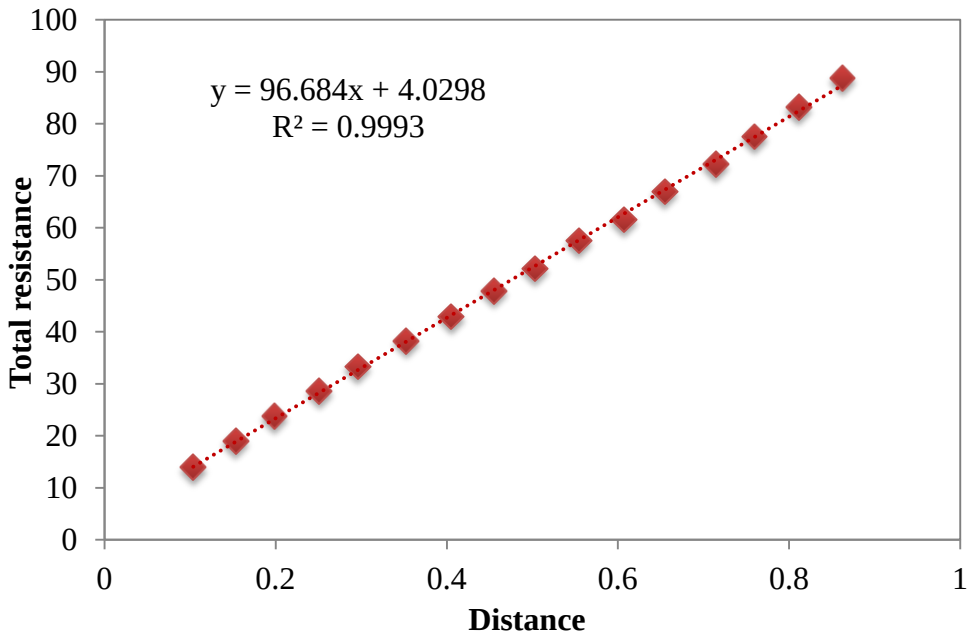


Figure 3.9: Measured resistances as a function of distance between TLM pads used for calculation of contact resistance

3.7 Conclusion

A spin-on diffusion process was studied and optimized to identify factors affecting the quality of the emitter. Optimal gas-flow was identified as an important factor for uniform emitter formation. In addition process was modified to include a short pre-oxidation step which resulted in emitters with higher uniformity and lower emitter saturation current density. This modified process was also found to be less sensitive to ambient humidity than earlier processes using spin-on commercial sources. Full Al BSF cells with screen printed contacts were fabricated with spin-on emitter and a peak efficiency of 19.6% was achieved. This represents the highest efficiency for a screen printed full BSF cells. Further analysis and characterization showed that a high quality in-situ oxide passivation of the emitter along with very good screen printed contacts contributed to this high efficiency.

This improved emitter and cell fabrication process was combined with local BSF and dielectric rear passivation in the following chapters. As discussed in chapter 2, this structure can achieve cell efficiencies over 20%. Subsequent chapters will discuss the design and fabrication of this advanced structure using the spin-on process developed in this chapter.

CHAPTER 4

FABRICATION OF ADVANCED CELL STRUCTURES

4.1 Introduction

In chapter 3, a spin-on process for forming an emitter was developed and applied to the fabrication of a high efficiency full Al BSF cell. The next step involves raising the cell efficiency further using an advanced cell structure with dielectric passivated local BSF cell. This involved the development of a high quality rear surface passivation and local BSF and contact. This chapter focuses on the fundamental understanding of this structure, technology development and fabrication of 20% efficient cells.

4.2 Understanding the Effect of Dielectric Charge on LBSF Cells

Local BSF cells provide a substantial advantage over full Al BSF due to the fact that over 90% of the rear surface is passivated using a dielectric which is superior to a full Al BSF. This contributes to both electrical and optical improvements in cell performance. There are many dielectrics that have been studied for passivation of the front and rear surfaces [83, 84]. The most common dielectric used in the PV and semiconductor industry for excellent surface passivation is thermal SiO_2. For example, the first crystalline silicon solar cells with efficiency exceeding 20% were fabricated using thick thermal oxide passivation at the University of New South Wales. These are known as the PERC and PERL cells [4, 5]. However, thicker oxides are not practical for mass production due to throughput issues, high thermal budgets and because they are not optimal anti-reflection

coatings for the front surface. Optimal AR coatings have a refractive index ≥ 2.0 to match with the glass cover in the module. Therefore, an alternative dielectric is needed that can be formed rapidly during diffusion at lower temperatures and can also provide high quality passivation and anti-reflection coating.

Fixed oxide charge and interface state density are critical parameters that dictate the surface passivation quality of a dielectric. In order to establish the requirements for the appropriate dielectric that can lead to 20% efficiency, a multi-dimensional simulation software, DESSIS^{TM}, was used by Meemongkolkiat in his thesis[82] to analyze the effect of fixed charge density in the rear dielectric on cell performance. His simulations assumed a device fabricated on a 200 μm thick 2 Ω.cm p-type substrate. An n^+ emitter with 75 Ω/□ sheet resistance was simulated on a textured front surface. The unit cell used in these simulations is shown in figure 4.1. Local rear contacts through the dielectric are formed to the Si using 75 μm × 75 μm squares with 1000 μm spacing. A 20 nm layer under the contact doped with B was used to simulate an ohmic contact. The results of the simulation can vary depending on the existence of a shunt path between the contact and the potentially induced inversion layer under the dielectric. Parasitic shunts can occur if the LBSF is pinched at the corner and Al metal is exposed to the inversion layer under the dielectric. This inversion layer is a side effect of the high positive charge in the dielectric, which can shunt the rear contact and lead to a loss in cell J_{SC} and efficiency [85]. Meemongkolkiat simulated this effect in the model by adjusting the work function of the metal used for the rear contact. A low work function of 4.1 eV allows the formation of a shunt path via tunneling through the 20nm dielectric and a high work

function of 5.2 eV turns off the shunt path [86]. The simulated solar cell efficiency as a function of fixed charge density is shown in figure 4.2. Also included in the figure are two visual guides showing the efficiency of these cells with no charge in the rear dielectric, but with surface recombination values of 0 cm/s and 1E6 cm/s, signifying the ideal dielectric and a metal contact, respectively.

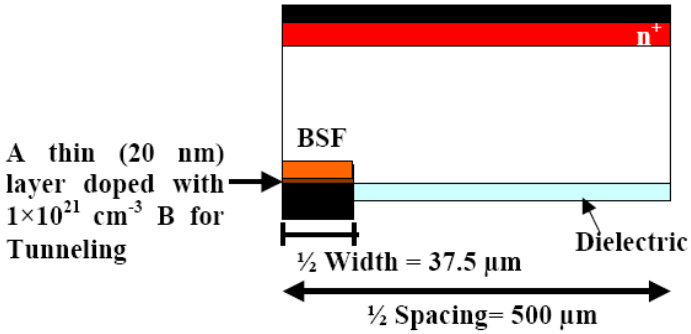


Figure 4.1: 2D simulation domain used to study the effects of rear dielectric charge on cell performance

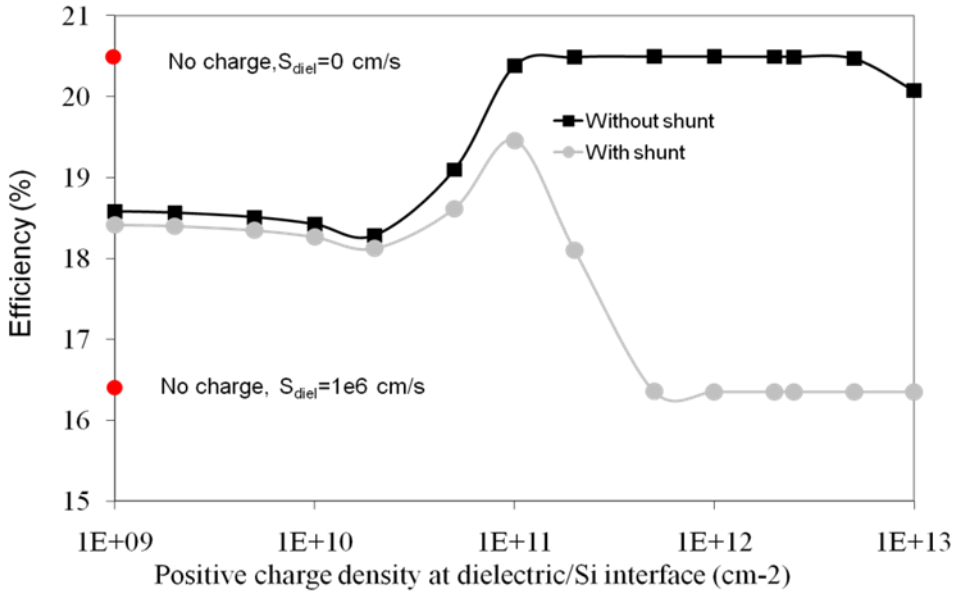


Figure 4.2: Results of 2D simulation showing the effect of high positive charge in the rear dielectric on cell performance

Meemongkolkiat's simulation results in figure 5.2 show that a high positive charge density, without a parasitic shunt, can provide a substantial improvement in cell efficiency (20%) by improving surface passivation. In this case, a wide range of positive charges can be accommodated in the rear dielectric without the loss in efficiency, making it a good choice for high efficiency cells. However, in the presence of a parasitic shunting between the local rear contact and the inversion layer, high positive charge in the rear dielectric becomes very harmful. It provides a modest improvement in efficiency up to a specific charge density of ~2E+11 cm^{-2} for the 2 Ω.cm substrate simulated in this study, but any further increase in the charge reduces the cell efficiency to 16%, which is worse than having no surface passivation. Meemongkolkiat concluded that optimal dielectric charge density is ~ 2E+11 cm^{-2}, with and without parasitic shunt, for a solar cell fabricated on 2 Ω.cm substrate. This reduces BSRV and also avoids strong inversion that could lead to parasitic shunting. Based on these guidelines, several dielectrics were compared in terms of charge and passivation [87]. This provided the guidelines to fabricate the appropriate dielectric and analyze it with respect to interface state density and charge. The charge density in the dielectrics was measured in this study using Semitest SCA 2500 Surface charge analyzer. The tool measures the flatband equivalent charge density (Q_{FB}) by a contactless and non-destructive method.

4.3 Investigation of Rear Dielectric and Al Contact Paste

Consistent with the above criteria, a rear dielectric stack composed of a commercially available spin-on glass, 20B, and PECVD SiN_x was developed and chosen for rear

passivation of a high efficiency cell structure. The spin-on glass was found to have optimum as-grown charge density of < 2E+11 cm^{-2} after annealing-induced oxidation. However when capped with the PECVD SiN_X, the net charge density in the stack increased to ~2E+11 cm^{-2}. According to the Meemongkolkiat's simulations, this charge can result in cell efficiencies over 20% when a parasitic shunt is avoided. Figure 5.2 shows that even in the presence of a parasitic shunt, this fixed charge density in the rear dielectric stack produces the peak cell efficiency for a base resistivity of 2 Ω.cm, Hence this dielectric stack was selected in this research, in combination with a specially designed Al paste [88] for fabrication of a high efficiency PERC type device. This Al paste could be screen printed over the entire rear surface similar to a full BSF device, but would only react with exposed Si within the vias to produce a local BSF. Al paste used in this study was fritless and consisted of 12% of Si by weight. The lack of a glass frit in the paste reduces the aggressive nature of the Al paste during the firing process. As a result, the rear passivation is not compromised during contact firing in regions surrounding the local BSF. The addition of 12 % of silicon is to supply extra silicon to aid the formation a thick and uniform BSF within the local vias.

During the fabrication of preliminary cells of this type, it was identified that the rear surface of the substrates would need to be completely planar and free of any diffusion to harness the maximum potential of this structure. To ensure this single side textured wafers were processed using a modified STAR process using spin-on phosphoric acid as the dopant source (as described in the chapter 3). The rear passivation was provided by

the spin-on glass and high efficiency cells were fabricated using the process described in subsequent sections.

4.4 Description of Process Sequence and Complete Cell Fabrication

In order to achieve 20% efficient solar cells, a LBSF cell structure called Delta-STAR was fabricated with a process flow shown in Figure 5.4. A source-target diffusion method called the STAR process, described in earlier chapters, was used. A dilute diffusion source with phosphoric acid, water and ethanol was developed [89] and prepared in-house for each process and spun-on the source wafer. The phosphoric acid solution used in this research had 1.25% of phosphorous by weight after dilution with water and ethanol. The commercially available spin-on dielectric, 20B, was spun over the planar rear surface of the target wafer and these two wafers were loaded in adjacent slots, as seen in figure 4.3, followed by a diffusion process at 925 ºC for ~5 minutes. The wafers were also oxidized for 5 minutes after the diffusion process ad then annealed in nitrogen ambient for 12 minutes, to gain a high quality oxide over the emitter and under the spin-on dielectric. The dilute spin-on phosphoric acid solution prevented phosphorous glass formation on the emitter and allowed for in-situ oxidation, which passivated both front and rear surfaces. This process resulted in 75 Ω/□ emitter with a thermally grown 100 Å passivating oxide on the front surface and ~2500 Å spin-on passivating oxide on the rear surface. It is important to note that all this was achieved in a single high temperature step.

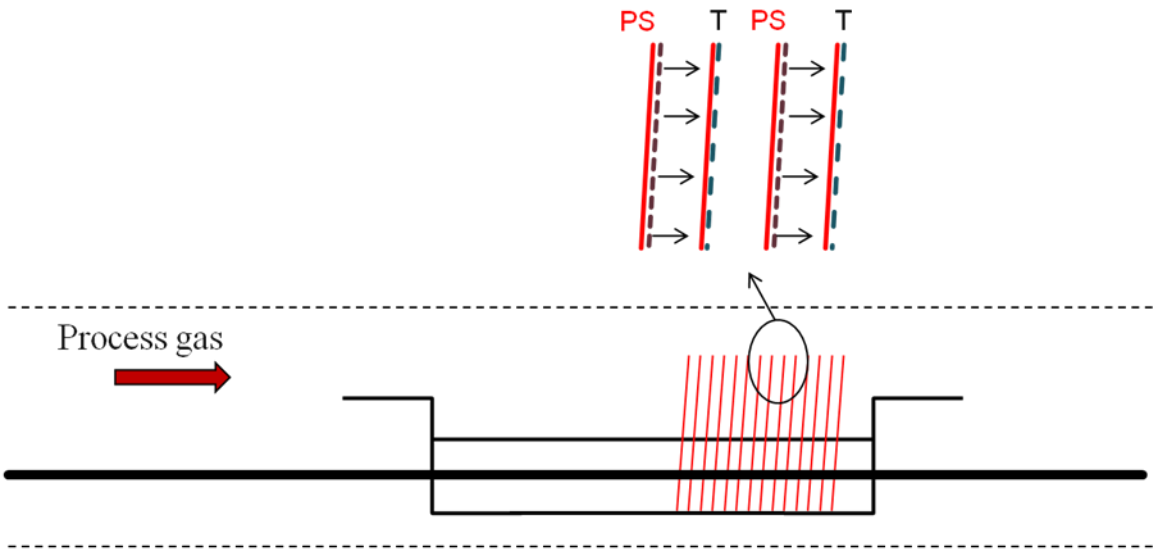


Figure 4.3: Schematic of loading sequence in diffusion tube for Delta-STAR process

Detailed characterization, discussed in subsequent sections, revealed that this process provided excellent front and rear passivation. The thick rear spin-on dielectric also masked the diffusion of phosphorous on the rear side. After that ~ 650 Å SiN_X coating was deposited on the front and rear using a standard low frequency PECVD process at 425 ºC. A screen-printing paste (from Merck KGAA) was used for the definition of vias through the rear dielectric. The vias were circular with a diameter of 100 µm and were spaced 800 µm apart. These optimized dimensions were obtained from simulation performed using DESSIS™, a two-dimensional modeling software [82]. Front Ag and rear Al contacts were screen printed and co-fired. The modified Al paste formed a local BSF through the vias, while the remaining areas had a dielectric stack capped with Al metal which provided good rear internal reflectance. A modified cell isolation technique involving dicing and chemical etching of nine 4 cm^2 cells was employed, followed by a forming gas anneal. During the modified isolation process, the wafers were coated with

photoresist prior to being isolated with a dicing saw. The exposed silicon with the isolation grooves were etched chemically to achieve a smooth isolation edge. This process reduced junction leakage currents caused by the isolation edge and hence, resulted in better FF, as discussed in chapter 3. A schematic of the process sequence and resulting cell structure is shown in figure 4.4 and 4.5, respectively.

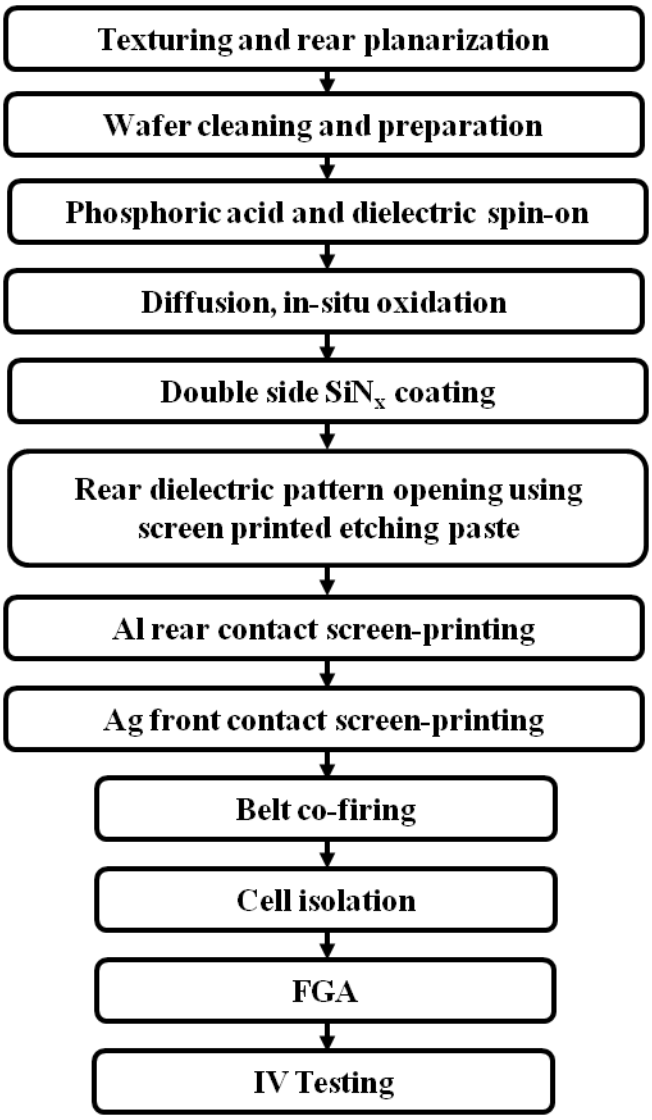


Figure 4.4: Schematic of process sequence used for Delta-STAR cell

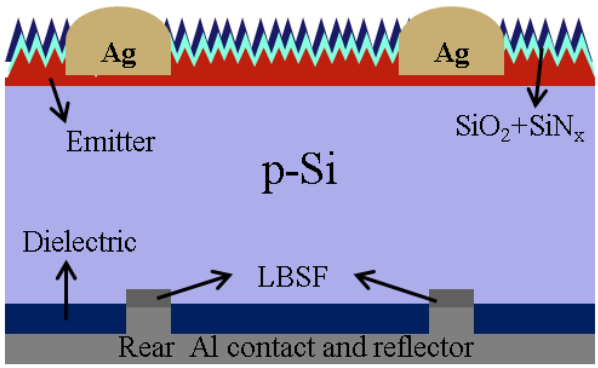


Figure 4.5: Schematic of Delta-STAR cell

4.5 Results and Analysis of Dielectric Passivated Local BSF Cells

The above process sequence was used to fabricate nine 4-cm^2 cells on 100 mm diameter, 300 µm thick FZ silicon wafers which had a base resistivity of 2.35 Ω.cm. Some baseline cells were also fabricated in the same experiment with full Al BSF structure with identical front passivation to serve as a reference or control. The resulting Delta-STAR cell had an efficiency of 20.1% while the best full Al BSF cell had an efficiency of 19.1%. It should be noted that this efficiency was lower than the best cells discussed in chapter 3, which were fabricated on 0.6 ohm.cm substrates. The difference in peak efficiency is attributed to the difference in substrate resistivity between the two studies. The best cells from both structures were tested and validated by NREL and can be seen in table 4.1.The LBSF cell showed an improvement in V_{OC} and J_{SC} compared to a full Al BSF cell fabricated on wafers of similar resistivity. The high V_{OC} was achieved from a combination of good front and rear passivation and was confirmed through detailed characterization of the cells. It should also be noted that the peak cell efficiency obtained

experimentally in this research matched very well with the simulated cell efficiency without a parasitic shunt resistance (Fig. 4.2). This suggests that the dielectric charge was sufficient to produce the benefits of field effect passivation without the formation of inversion layer and parasitic shunting. This improved passivation resulted in a high J_{SC} and cell efficiency.

Table 4.1: Results of IV testing performed at NREL*

Cell	Voc (mV)	Jsc (mA/cm^2)	Efficiency (%)	Fill Factor (%)
Delta-STAR	652	39.4	20.1	78.1
Full BSF	639	37.9	19.1	78.9

* - Cell data as with a 3.8 cm^2 aperture mask

4.6 Characterization and Modeling of 20% Efficient Delta Star Cells

The finished solar cells were characterized to obtain the reflectance and Internal Quantum Efficiency (IQE) data to quantify the benefit of dielectric passivation and local BSF. The IQE data was collected for wavelengths in the range of 300 – 1200 nm at 10 nm intervals. This was used to compare the short and long wavelength responses to see the effect of the dielectric front and rear passivation. Dark IV measurements were also performed on the best cells to extract contact and junction parameters. The two types of devices, baseline and Delta-STAR, were modeled using PC1D to fit the cell data and extract relevant cell parameters. Modeling was performed with 300 μm thick wafers and resistivity of 2.35 Ω.cm. Dielectric passivation of the rear surface was modeled using the measured charge

in the rear dielectric layer of this structure. The measured and modeled IQE and reflectance curves for both cells can be seen in Figure 4.6. Table 4.2 also lists the parameters extracted from modeling and characterization.

Both full Al BSF and Delta-STAR cells had a ~75 Ω/□ emitter that was passivated with a thin (~ 100 Å) thermal oxide. A PC1D model fit to short wavelength IQE response gave an FSRV of ~13000 cm/s. However the long wavelength response of the dielectric passivated LBSF cells was found to be much better than the Al BSF cells (Fig. 5.6). The BSRV value obtained by fitting the modeled and the measured long wavelength IQE curves of the two cells gave a BSRV value of 325 cm/s for the full Al BSF cell and 125 cm/s for the local BSF cell (Fig 4.6). Comparison of the escape reflectance curves (λ >1100 nm) for the two different cell structures clearly indicates an improved back surface reflectance (BSR) value for the Delta–STAR cell. PC1D modeling of long wavelength IQE (λ > 1050 nm) revealed that the spin-on oxide/Nitride stack passivation with Al metal cap improved the BSR to 93% relative to the BSR value of 67% for the full Al BSF cell.

Table 4.2: Cell parameters used in modeling

Parameters		Dielectric back	BSF back	Acquiring method
BSRV ($S_{n0}=S_{p0}$) (cm/s)		125	325	From IQE Fit
FSRV ($S_{n0}=S_{p0}$) (cm/s)		13,000	13,000	From IQE Fit
Bulk lifetime ($\tau_{n0}=\tau_{p0}$) (μs)		1,000	1000	Measured on Adjacent wafer without metal contacts
Front internal reflection (Specular) (%)	1st bounce	84	93	
	Subsequent bounce	92	93	
Back internal reflection (Diffused) (%)	1st bounce	93	67	From escaped reflectance fit
	Subsequent bounce	90	67	
Series resistance (ohm-cm^2)		0.66	0.49	Light I-V measurement
Shunt resistance (ohm-cm^2)		8083	2666	
Charge in the rear dielectric (cm^{-2})		1.4×10^{11}	N/A	Measured/ I-V fit
Front surface		Textured: angle 54.74°, depth 3.535 μm		Assumed
Front reflectance		From measured data with escaped reflectance removed		Measured reflectance
Substrate		300 μm, ρ=2.35 Ω-cm		Measurement
Emitter profiles		Measured data		Spreading resistance measurement

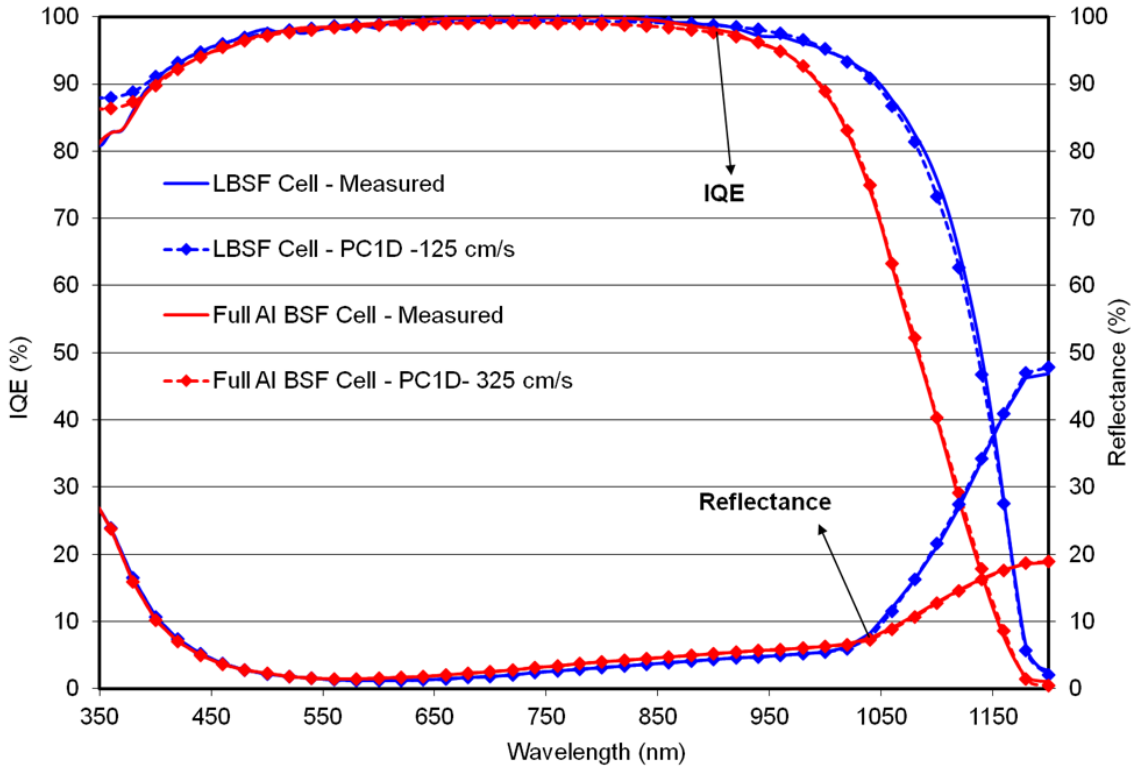


Figure 4.6: IQE and reflectance comparison of the two cells

4.7 Characterization of Passivation Quality of Spin-On Dielectric

The passivation quality of the spin-on oxide/nitride stack passivation was also evaluated in a separate experiment by applying the spin-on dielectric on both sides of 300 µm thick 2.3 ohm.cm planar wafers and then subjecting them to the anneal process identical to cell wafers. Note that there was no phosphorous diffusion performed on these wafers. Silicon nitride film was then deposited on both sides using a low-frequency PECVD process. These wafers were subjected to a contact firing thermal cycle and annealed in forming gas similar to the actual cells. Thus the wafers received identical thermal budget but without the diffusion and metal contacts. Effective lifetime (τeff) measurements were

made at each stage to evaluate the quality of passivation using a PCD lifetime tester. Results of these measurements are shown in figure 4.7. Surface recombination velocity (S) was obtained using the equation

$$\frac{1}{\tau eff} = \frac{1}{\tau bulk} + \frac{2S}{L} \qquad \ldots\ldots. (4.1)$$

where L is the wafer thickness and $\tau bulk$ is the bulk lifetime (1 ms). These calculations reveal that the dielectric stack alone is capable of reducing BSRV to <50 cm/s. Since PC1D matching gave an effective BSRV of 125 cm/s, it suggests that contact recombination increased the net BSRV from 50 to 125 cm/s.

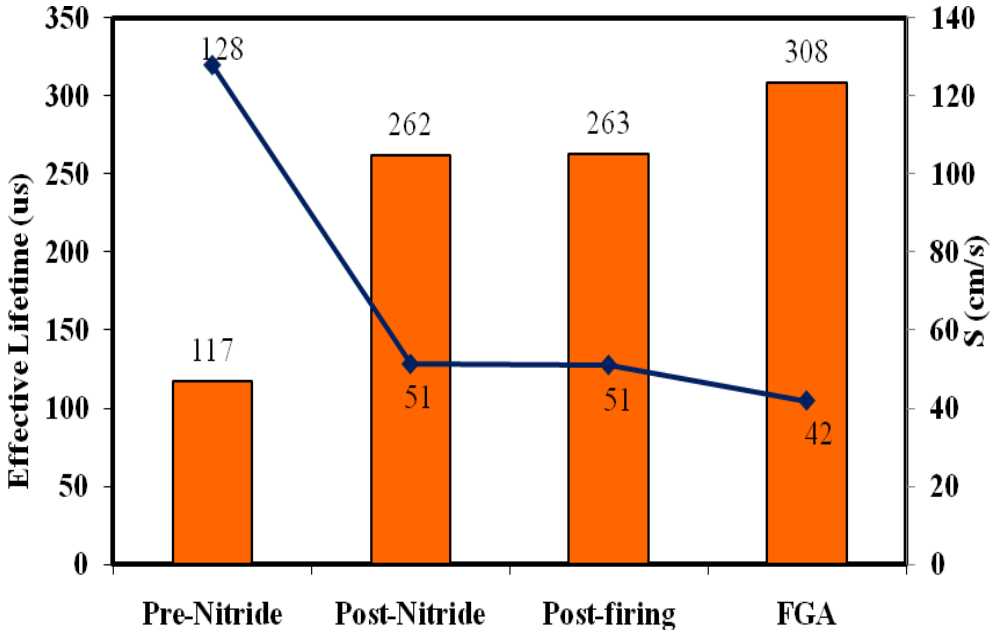


Figure 4.7: Measured effective lifetimes at various stages of processing

4.8 Extended Characterization of High Efficiency Delta-STAR Cells

To enhance the quantitative understanding of our 20% efficient cell, an analytical solution developed by [90] was applied. Fischer's work provided an equation for calculating the effective SRV for rear passivated cell structures.

$$Seff = \frac{De}{W}\left(\frac{Lp}{2W\pi f}\arctan\left(\frac{2W}{Lp}\sqrt{\frac{\pi}{f}}\right) - \exp\left(-\frac{W}{Lp}\right) + \frac{De}{fWSmet}\right)^{-1} + \frac{Spass}{1-f} \quad (4.2)$$

,where S_{eff} is the effective SRV of the combined effect of the metalized regions and the dielectric passivated area of the rear surface, S_{met} is the surface recombination velocity at the metal/BSF interface, S_{pass} is the recombination velocity at the dielectric-Si interface, D_e denotes the diffusion constant of the minority carriers, f is the metal contact fraction (< 5%), L_p is the contact pitch (~800 µm) and W is the thickness of the substrate.

Using the measured parameters for the 20% cell in this study in conjunction with the modeled BSRV (S_{eff}) of 125 cm/s and measured S_{pass} of 42 cm/s, S_{met} was calculated to be ~ 30000 cm/s. This value is comparable to the S_{met} calculated in another study on similar PERC type cells [91], suggesting that the recombination at the interface of the local BSF and silicon substrate is similar.

The combination of all these factors resulted in a net 1% improvement in cell efficiency of local BSF cell compared to the full Al BSF cell. The contributions from the two improvements were modeled using the PC1D model for the full Al BSF cell. BSR was increased from 67% to 93% in the model to calculate the impact of BSR. Separately, the BSRV was changed from 325 cm/s to 125 cm/s in the PC1D model to quantify the

contributions from rear surface passivation. Each of these two improvements contributed ~0.5% (absolute) in efficiency improvement over a full Al BSF cell. The quantitative assessment of efficiency enhancement due to various factors is shown in figure 4.8. The difference in fill factor is predominantly an effect of the slightly higher series resistance in Delta-STAR cells due to rear point contacts as opposed to a full metal contact. Detailed analysis of the cell through characterization and simulation revealed that the passivation quality of the spin-on dielectric is comparable to that of a good thermal oxide due to field effect passivation. In addition, the in-situ oxidation after diffusion may grow a high quality thin thermal oxide underneath the spin-on dielectric. The thickness of the dielectric layer (~2500 Å) helped in partially decoupling the higher positive charge of the SiN_X to prevent inversion and parasitic shunting. Hence, the cell IV characteristics of the spin-on dielectric cells in this study are similar to those reported for thermal oxide passivated cells in literature [3,4].

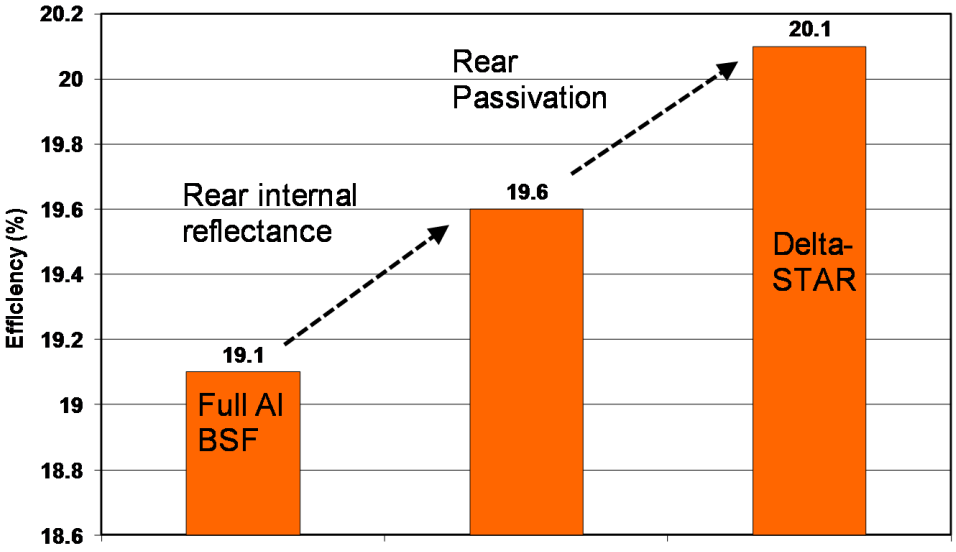


Figure 4.8: Effect of various factors on efficiency

4.9 Evaluating Benefits of Limited Source Diffusion Compared to $POCl_3$ Diffusion

While these experiments revealed the peak efficiency of 20%, experiments were performed to identify the benefits of this simple process involving a single high temperature process. For example, an alternate processing scheme to fabricate the similar devices using conventional $POCl_3$ diffusion process would have resulted in a deposition of a thick diffusion glass on the target wafers, which would have required chemical etching before subsequent processing. This chemical process would also remove any in-situ passivating oxide grown during the diffusion process. As a result, any process using the $POCl_3$ diffusion for the formation of emitters would require a second high temperature process for growing a passivating oxide on the front surface and annealing the rear dielectric. Local BSF cells were also fabricated in this study using the $POCl_3$ process to compare its performance to the simple 1-step process developed in this reaearch. A schematic of the 2-step process is provided in figure 4.9 and the results from the two processes are summarized in Table 4.3.

It is clear that the peak and average cell performance was superior for the single step process developed in this research. While the cell V_{OC} did not show a significant difference, the low FF and J_{SC} suggest that parasitic shunts may be responsible for the loss in performance for cells fabricated using the 2-step process. This could happen if the rear dielectric does not serve as a perfect mask for $POCl_3$ diffusion and localized diffusion of P at the rear surface would lead to parasitic shunts and low cell performance. In the case of our single side limited source diffusion process with a thick spin-on rear

dielectric, there was adequate protection to prevent any phosphorous diffusion on the rear side.

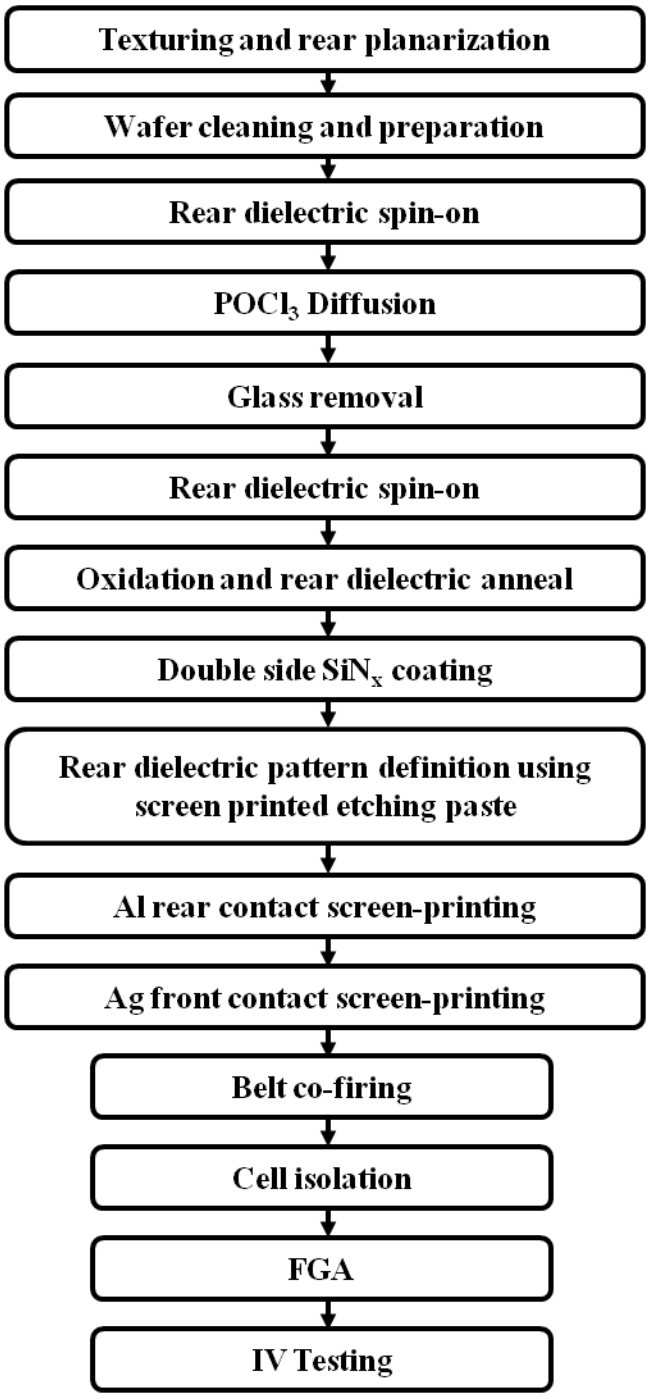


Figure 4.9: Schematic of process sequence using 2 high temperature steps for LBSF cell fabrication

Table 4.3: Summary of results comparing LBSF cells from two different processing routes

Process		Voc (mV)	Jsc (mA/cm²)	Eff (%)	FF(%)
1 Step	Best	661	38.8	20.3	80.6
1 Step	Average	657	38.1	19.6	78.2
2 Step	Best	663	37.8	19.7	79.3
2 Step	Average	653	37.1	18.5	77.3

To validate that this performance difference was from the rear of the cell, full Al BSF cells were fabricated with the spin-on and $POCl_3$ emitters. On analysis of the peak and average values of the vital cell parameters, it was observed that both processes resulted in similar cell V_{OC}. The difference in J_{SC}, between cells fabricated using 1-step and 2-step processing, was < 0.5 mA/cm^2 on average, which was significantly less than that seen on LBSF cells. This reduced difference resulted in comparable cell efficiencies for cells by the two processing routes. These observations led to the conclusion that the significantly inferior performance of $POCl_3$ diffused cells was not related to the emitter or front surface passivation but was caused by parasitic shunting. Thus, it was concluded that the 1-step using spin-on diffusion, not only results in a shorter and simpler process with a lower thermal budget, but also produces better cell efficiencies by minimizing parasitic shunting.

4.10 Comparison of Passivation Quality of the Spin-On Dielectrics to Thermal Oxide

Previous sections showed that a spin-on dielectric was used successfully in combination with in-situ oxidation to achieve high quality rear surface passivation and 20% efficient cells. However, thermal oxide is the simplest dielectric for surface passivation, which typically has a fixed charge of < 2E+11 cm^{-2}. However, thermal oxides cannot be used for rear passivation by themselves for screen printed cells because thermal oxides can not retain passivation quality when subjected to a high temperature contact firing process (700 – 800 ºC in air). As a result, a PECVD SiN_x cap is generally used to protect the oxide and preserve passivation. The PECVD SiN_x cap increases the net charge of the dielectric stack to > 1E+12 cm^{-2}. Local BSF cells were fabricated with this dielectric stack providing rear passivation. Two different thicknesses of thermal oxides (90 Å and ~750 Å) and were grown on the rear surface to compare cell results. Process sequences are shown in figures 4.10a and 4.10b. The results of these experiments are shown in table 4.4.

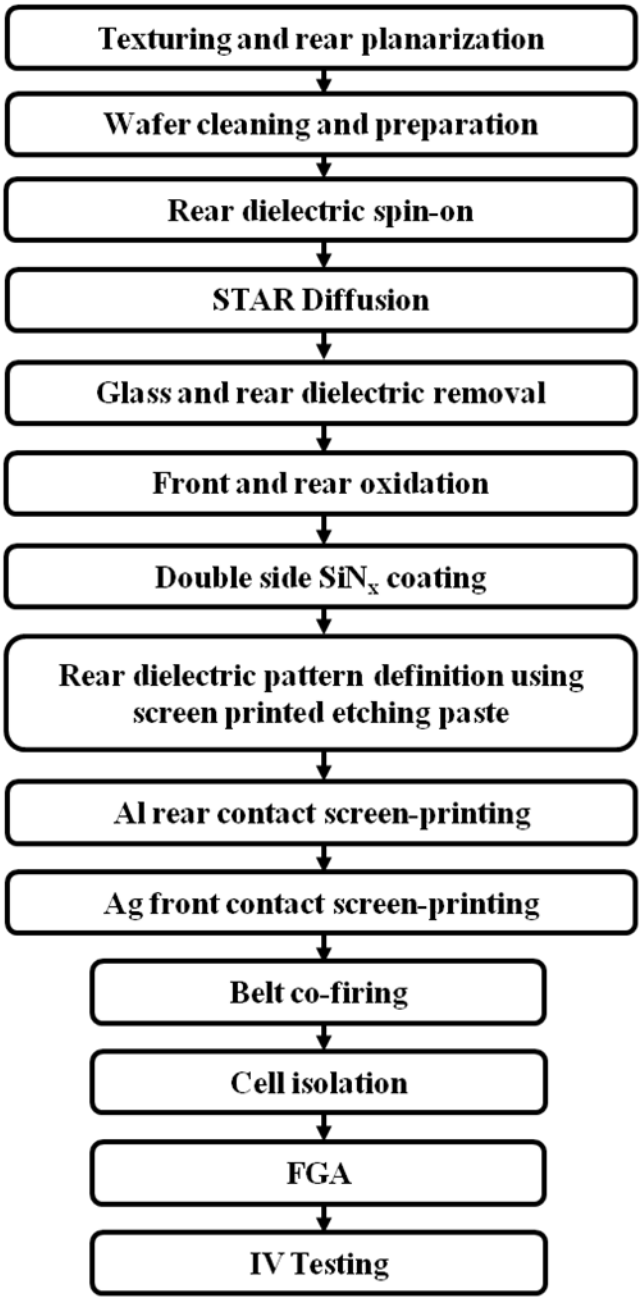


Figure 4.10a: Schematic of process sequence used for fabrication of cells using thin oxide/SiN_X stack for rear passivation

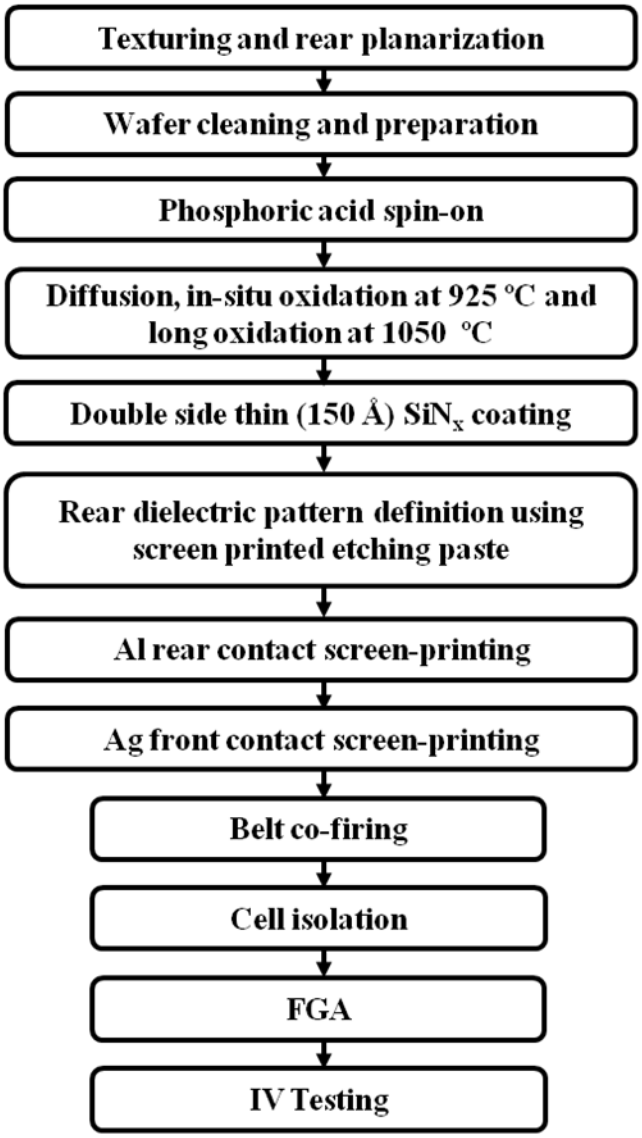


Figure 4.10b: Schematic of process sequence used for fabrication of cells using thick oxide/SiN_X stack for rear passivation

Table 4.4: Peak efficiencies of cells with different dielectric stacks for rear passivation

Rear Dielectric	Oxide Thickness	Voc (V)	Jsc (mA/cm²)	Eff(%)	FF (%)
20B/SiNx	2500 Å	**0.652**	**39.4**	**20.1**	**78.1**
Thin thermal Oxide/SiNx	90 Å	**0.645**	**38.4**	**19.2**	**77.5**
Thick thermal Oxide/SiNx	750 Å	**0.621**	**36.3**	**17.6**	**78.2**

It was clear that spin-on dielectric with single side diffusion was superior to both thin and thick thermal oxide passivation. To understand the reasons for this, the best cells were characterized using IQE and reflectance measurements. As seen in figure 4.11, the Delta-STAR cells with a 20B/SiNx rear stack exhibited the best long wavelength (900-1050 nm) response. In addition, the long wavelength response of cells with thermal oxides on the rear surface revealed an inflection – or a "kink" that is a charscteristic of parasitic shunt [23] resulting from the high fixed charge in the dielectric in proximity to the silicon surface. The long wavelength response of the thick oxide passivated device was found to be significantly lower, indicating that the long oxidation process may have also degraded the bulk lifetime. These cells also had the lowest reflectance of the three structures, which could be partly responsible for their lower J_{SC}, because these cells had a thick oxide, on the front, capped with a thin SiN_X for anti-reflection coating. Thus, the dielectric stack of 20B/SiN_x with spin-on Phosphorous diffusion offered passivation performance that was

superior to those with thermal oxides, besides enabling simple and elegant cell fabrication.

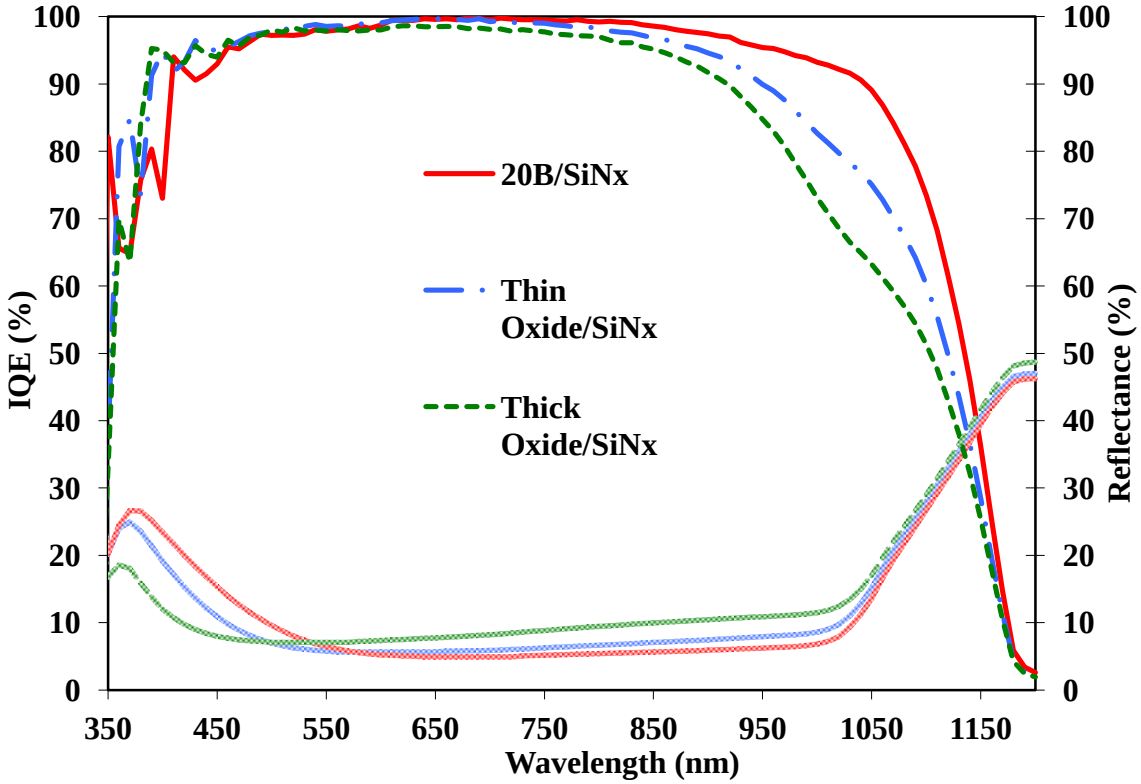


Figure 4.11: Comparison of IQE and reflectance of cells with different dielectric stacks

4.11 Investigation of Alternate Spin-on Dielectric Solutions

Based on the success of using commercial spin-on dielectrics, alternate polymeric dielectrics were also investigated using the spin-on processing. One such candidate was polymeric hydrogen silsesquioxane (HSQ). This polymeric dielectric is used commonly as a dielectric in the IC industry and can results in very uniform step coverage. When the HSQ polymer is annealed at high temperatures (~800 ºC), it converts to a SiO_2-like

structure through the decomposition of HSQ [92]. Since the end product was a passivating oxide similar to that obtained from the earlier commercial solution, a more detailed investigation was undertaken for the use of this dielectric with a PECVD SiNx for rear passivation of high efficiency Delta-STAR devices.

After the spinning of the dielectric, the wafers were annealed in a furnace. Three different annealing conditions were considered:

i) A short oxidation (SO) anneal consisting of a rapid heating to temperatures > 800 ºC and a very short dwell time (~2 secs) at the peak temperature

ii) A long oxidation (LO) anneal process consisting of a more gradual heating up to 650 ºC, followed by a faster ramp-up to temperatures > 800 ºC and a very short dwell time (~3 secs) at the peak temperature

iii) A combination of two short oxidation anneal steps similar to (i) – SO + SO

These processes were performed on two sets of identical wafers coated with dielectrics - one set designated for local BSF cell fabrication and the other set of wafers, symmetrically coated for measurement of effective lifetimes and passivation quality. These wafers were to be processed with a reference samples coated with the standard spin-on dielectric, 20B.

After fabrication of local BSF and full BSF cells, it was noted that wafers which were processed using a combination of 2 short anneals resulted in the best cells. However, the cell efficiency on these wafers was still inferior to the cells that were passivated with 20B and at best were comparable to the passivation offered by a full BSF. Both cell V_{OC} and

J_{SC} were significantly worse for all cells with the HSQ-based rear passivation. This indicated that the passivation provided by the HSQ dielectric was inferior to that of 20B. To confirm this, long wavelength (980 nm) LBIC responses of the typical cells were compared. The trends in average LBIC responses matched quite well with those in actual cell performance indicating that the quality of rear passivation was very closely tied to the anneal process.

4.12 Optimization of HSQ Dielectric Thickness

Based on the cell results of the previous experiments, it was observed that the cell J_{SC} and FF were much lower than those of typical Delta-STAR cells. These results did not correlate with the IQE and reflectance measurements that showed these cells should have had performance identical to the best Delta-STAR cells. This mismatch was an indication of inversion caused by the charge in the dielectric. In addition, the lower fill factors were also partially attributed to the use of substrates with resistivity higher than the earlier studies. As a result, subsequent experiments were performed on standard resistivity substrates to optimize the thickness of the dielectric and to maximize passivation.

Based on earlier experiments with the thick thermal oxides, it was decided that thicknesses > 1000 Å would be analyzed with at least one dielectric thickness comparable to the standard 20B dielectric used. HSQ dielectrics with three different thicknesses were chosen for further experiments. The measured average thicknesses of the three dielectrics were in the range of 1700 Å, 2700 Å and 4000 Å. As with the earlier experiments, separate sets of wafers were coated with each dielectric and used for cell fabrication and

study of passivation. Selected results from cell fabrication can be seen in table 4.5. As with the earlier experiments, none of the three dielectrics had a surface recombination velocity that was as low as the standard dielectric, 20B. A more detailed analysis of the dielectrics was necessary to understand the reasons for this.

Table 4.5: Results of light I-V testing of HSQ dielectric passivated LBSF cells

Cell type	Voc (mV)	Jsc (mA/cm²)	Eff(%)	FF (%)
Standard - 20B	0.653	39.1	19.6	76.8
HSQ - 4000 Å	0.642	37.9	18.8	77.2
HSQ - 2700 Å	0.643	38.3	19.3	78.4
HSQ - 1700 Å	0.643	38.6	19.4	78.3
Full BSF Reference	0.645	37.4	18.6	77.0

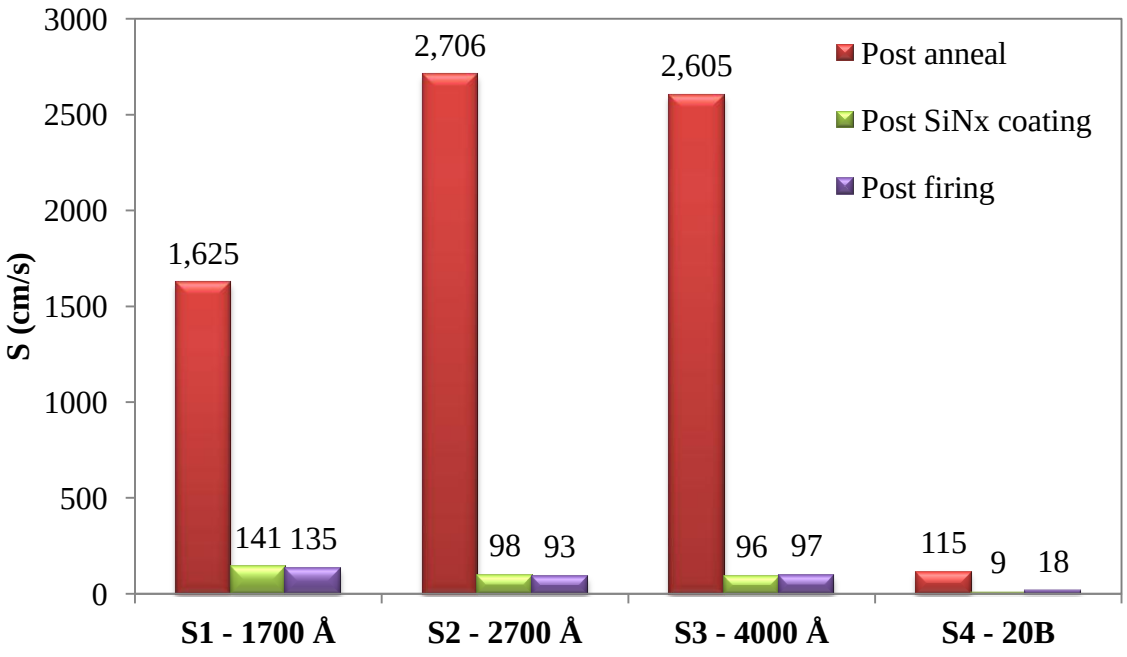


Figure 4.12: Characterization of progress of dielectric passivation with processing

4.13 Characterization of HSQ Dielectric to Identify Future Improvements

Charge measurements were made using a SemiTest SCA-2500 Surface Charge Analyzer on all HSQ dielectrics and standard dielectric, 20B. The measured values can be seen in figure 4.13. It should be noted that there was a significant difference in charge between the 2 dielectrics but there appears to be no dependence of charge on thickness of the HSQ dielectric.

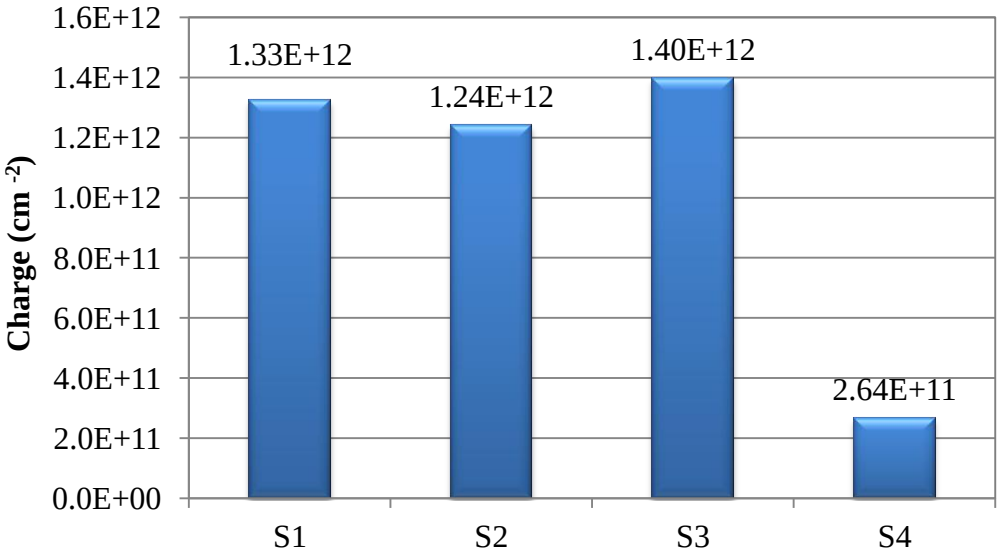


Figure 4.13: Measured charge on 4 wafers comparing HSQ and 20B dielectric

Interface states (D_{it}) were measured next to characterize the dielectrics further. A lower D_{it} value leads to better passivation. This value was also measured using on all four samples. However since the standard dielectric had a very low value it, a related parameter, called Interface Quality Factor (IQF), was measured on the four samples. A lower value of IQF indicates a better interface quality and the definition of IQF can be seen in equation 4.3 [93]. The chart below in figure 4.14 plots both D_{it} and IQF for the

four samples. A low D_{it} value was assumed for the GT dielectric based on literature. As seen from the trends, as thickness of the HSQ dielectric increases, the IQF and D_{it} decrease, resulting in a better passivation.

$$IQF = \frac{1}{qN_{SC}} \frac{dQ_{ind}}{dW_d} \qquad \text{..... (4.3)}$$

where, Q_{ind} is the induced charge, W_d is the width of the space charge region and N_{SC} is the substrate doping density of the semiconductor wafer.

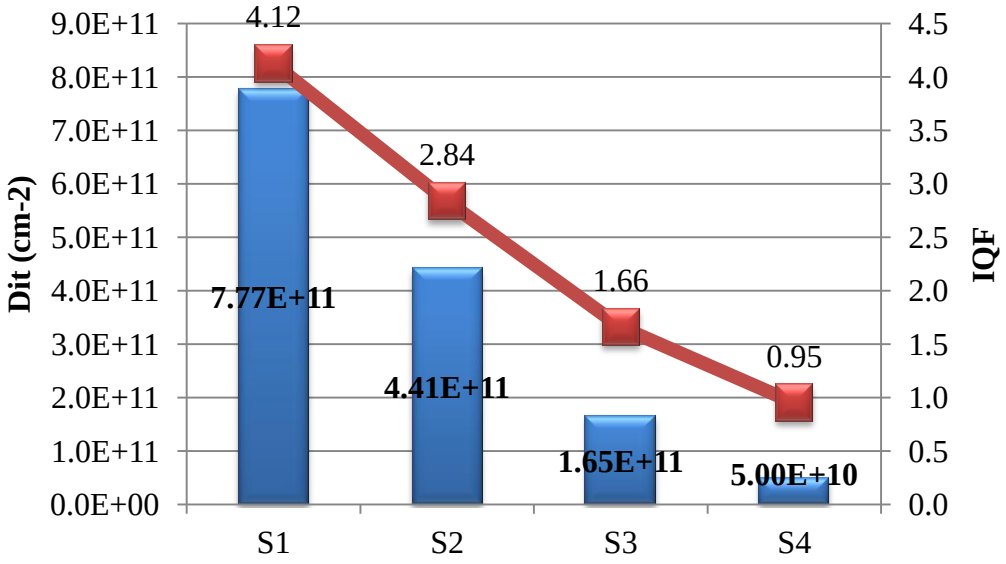


Figure 4.14: Measured values of D_{it} and IQF on HSQ and GT dielectric

These measured values of charge and Dit were used in model to calculate the resulting value of the recombination velocity, S, as a function of injection level for samples S2 and S4, where S2 was 2700 Å thick HSQ dielectric and S4 was 20B, the reference Georgia Tech dielectric. This can be seen in figure 4.15 below. The difference in modeled S values is comparable to those measured in earlier characterization and is considered the main reason for the inferior results obtained on the cells fabricated using these dielectrics.

In spite of the higher charge and higher D_{it} of the HSQ dielectrics, an optimal anneal process and thickness were identified which resulted in cell efficiencies of ~19.5%. An improvement in D_{it} is vital to the improvement of the HSQ dielectric. Future work towards such improvement could result in the cell efficiencies over 20% fabricated using a completely spin-on based process.

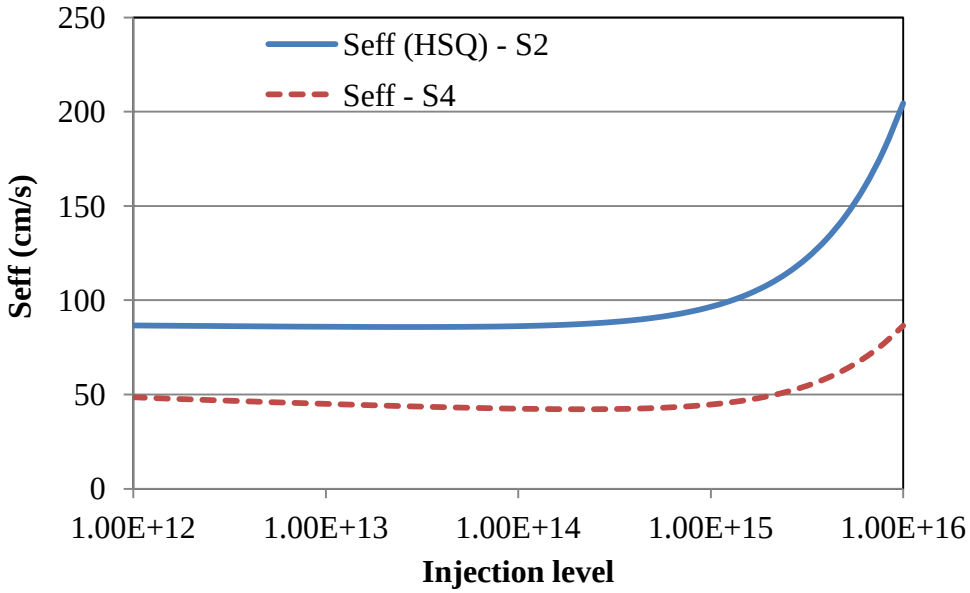


Figure 4.15: Modeled S as a function of Injection level

4.14 Conclusions

In this chapter, the various factors that are relevant to fabrication of high efficiency local BSF cells were addressed. Based on these initial studies, a local BSF design was implemented using a single side spin-on Phosphorous diffusion for the emitter and a spin-on dielectric for rear passivation. A simple and elegant process sequence was designed to produce a high quality 75 Ω/□ emitter on the front and rear passivation simultaneously in only one high temperature step. This 1-step process resulted in peak cell efficiency of

20.1% with an improvement in absolute efficiency of 1% over the conventional full BSF cells. Complete characterization and analysis was performed to identify the contributions from rear passivation and improved rear reflectance. The BSRV value decreased from 325 cm/s for a full Al BSF cell to 125 cm/s for the dielectric passivated local Al BSF cell. In addition, BSR improved from 67% to 93% due to the dielectric layers between the silicon and the rear contact metal. Modeling revealed that ~0.5% increase resulted from improved passivation and ~0.5% from improved rear reflectance. It was also shown that this streamlined 1-step process using spin-on phosphorous source resulted in better performance than double-side $POCl_3$ diffused cells because of parasitic shunting associated with inadequate masking of the rear surface during $POCl_3$ diffusion. Cells fabricated using the spin-on process were found to be superior to cells passivated with thin (90Å) and thick (750Å) thermal oxides. The thick spin-on dielectric decouples the effect of the high positive from the rear surface, leading to lower inversion and parasitic shunting. Alternate spin-on dielectrics based on HSQ were also studied for use in these cell structures, which resulted in peak efficiencies of ~19.5%. Further optimization of charge and Dit in HSQ dielectrics may lead to > 20% efficient cells with this spin-on dielectric also.

CHAPTER 5

LASER PROCESSING OF ADVANCED CELL STRUCTURES

5.1 Introduction

Earlier chapters in this work have discussed the development of a spin-on process for diffusion, which when combined another spin-on dielectric on the rear can lead to a local BSF cell with a single high temperature step. The process flow and fabrication parameters were optimized to demonstrate a peak efficiency of 20%. This peak performance was achieved on thick, high bulk lifetime wafers using laboratory scale processes. This chapter addresses some non-uniformities observed with those processes. To improve the process consistency, precision and throughput, laser processing is investigated in this chapter as an alternative to screen printed etching paste for dielectric ablation. Various laser candidates were investigated and results of characterization and successful fabrication of 20% cells is repeated in this chapter.

5.2 Analysis of Non-uniformities in LBSF Cell Processing

In order to benefit from the high quality passivation due to high positive charge in the rear dielectric, inversion layer related parasitic shunts have to be avoided [94]. The significance of parasitic shunting was discussed in Chapter 2. In the PERL cell, parasitic shunts were avoided using a larger area of local Boron diffusion under the smaller area of the contact. With this design, the metal has no contact with the inversion layer underneath the surrounding dielectric, even if it is present. In this particular cell structure, the LBSF

formed as a result of the firing the aluminum paste through the vias is expected to be the isolation between the Al contact and any inversion layer formed under the surrounding dielectric. The absence of a uniform BSF around the contact provides a parasitic shunt path for the minority carriers to flow through the inversion layer into the contact and hence results in a loss of cell performance. The doping level of this BSF also needs to be high enough to minimize the parasitic shunt.

In an earlier doctoral work, it was suggested that this parasitic shunt path can be modeled in PC1D as a shunt resistor or a diode of a suitable value (seen in figure 5.1). The value assigned to this parameter varies depending on the extent and the kind of contact between the rear metal and inversion layer. A lower than optimal doping level of the BSF might result in only a mild shunt. However a direct contact between the metal and the inversion layer with no BSF isolation between the two would result in a significant loss of cell performance. The comparison the two operating states – with and without parasitic shunts - can be seen in Figure 5.2 as a result of PC1D simulations performed with and without a parasitic diode. It should be noted that for a sufficiently severe shunt, the cell performance can degrade so significantly that the benefits of the high quality passivation are lost and the cells can be inferior to a similarly fabricated full Al BSF structure. This is an inherent risk with this device and needs to be addressed to harness the full potential of this cell structure.

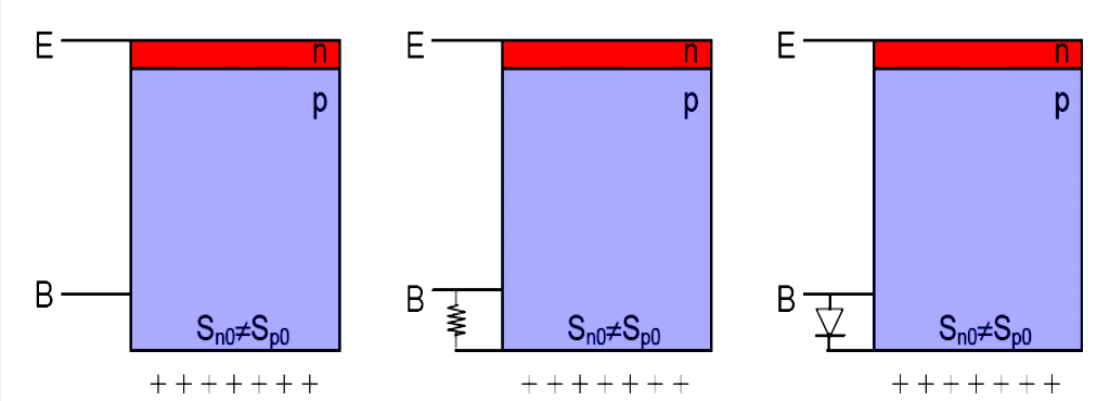


Figure 5.1: Schematic of cell structure used to model rear parasitic shunts in LBSF cells

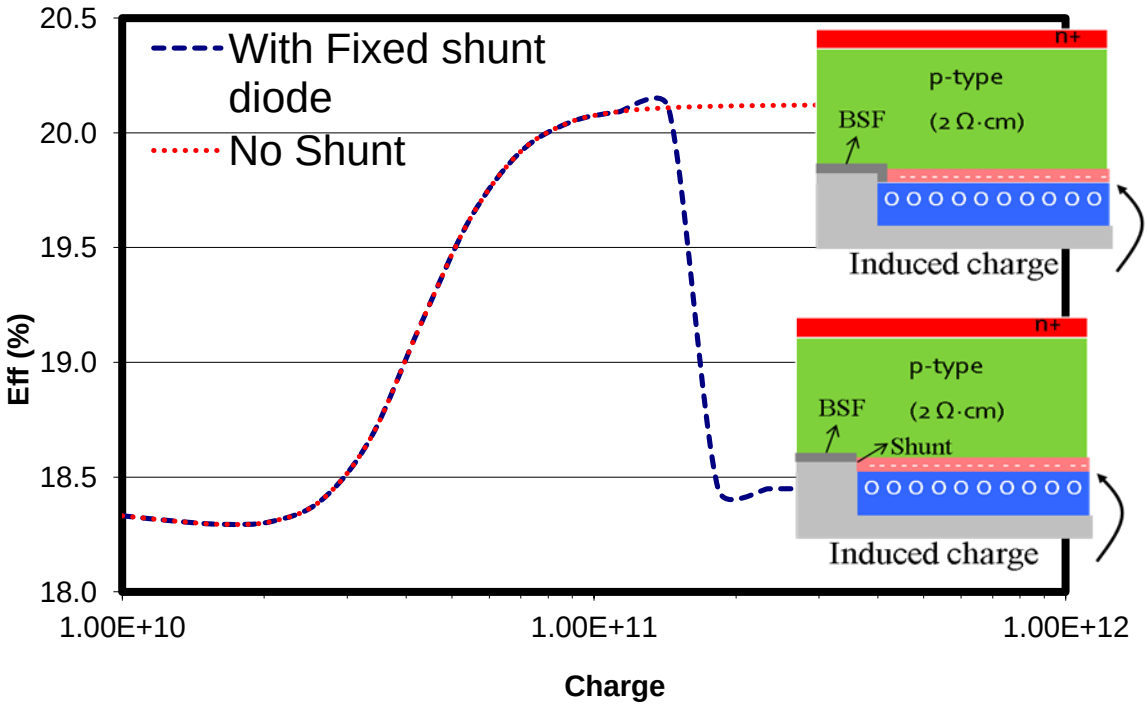


Figure 5.2: Results of PC1D simulation with and without a rear parasitic shunt

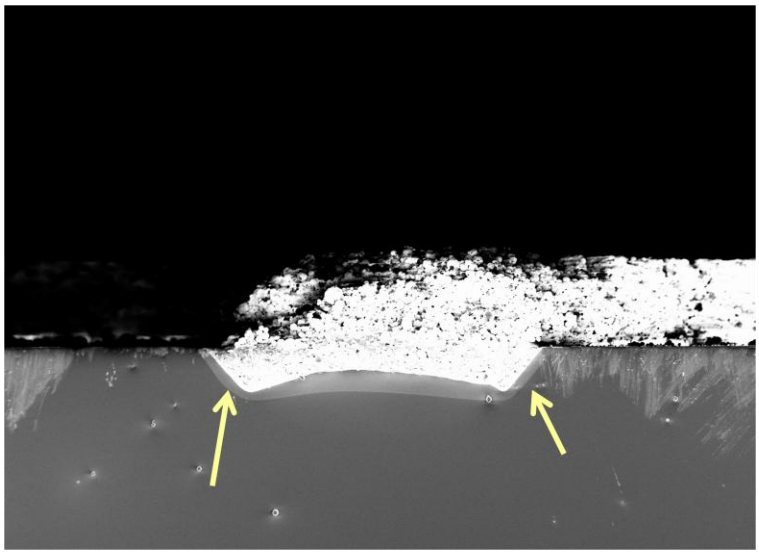
In this work, 20% efficiency on 4 cm^2 cells was achieved with a low-cost screen printing technology. Via definition was performed using an etching paste that required a 45 second baking step on a hot plate to facilitate the etching reaction. This step was found to

be very sensitive to the wafer thickness and thickness of the dielectric. Any non-idealities during processing could give rise to incomplete definition of vias. In addition paste spreading as a result of the screen-printing process would also partially etch the dielectric surround the actual via. Both these side-effects of using a screen-printed paste for via definition can result in a non-uniform BSF formation that could lead to parasitic shunts between the contact metal and the inversion layer. In a wafer with thousands of such vias, even a few shunted contacts could adversely affect the performance of the entire wafer. In addition, these process variations cause deviations from designed contact geometries and affect reproducibility of high efficiency.

5.2.1 Experimental Observation of Non-uniformities in LBSF Formation

Some of the aforementioned variations were observed in early iterations of this fabrication process. Some cells had efficiencies very close to the peak value, while others had efficiencies < 18.5 % when all other processing was identical. To verify if this was an effect of parasitic shunting, cross sections of the local contact and BSF were observed using scanning electron microscopy (SEM). Representative cases from two extreme cases of cell performance are seen in figure 5.3. Figure 5.3(a) shows a thick local BSF seen as a bright band surrounding the metal contact. It should also be noted that the shape of the local BSF and local contact are typical of those observed in high efficiency cells and the measured contact width shows minimal deviation from designed dimensions. However, in figure 5.3(b) it can be seen that the local contact has a non-uniform shape. This is believed to be because of non-uniform etching of the dielectric by the paste around the circumference resulting in rear Al firing to go through in these regions to make contact

directly with the Si. In the figure 5.3(b), closer inspection of this region, indicated by the arrows, reveals no BSF formation. This is experimental evidence of parasitic shunting that confirms the earlier simulations and needs to be avoided.



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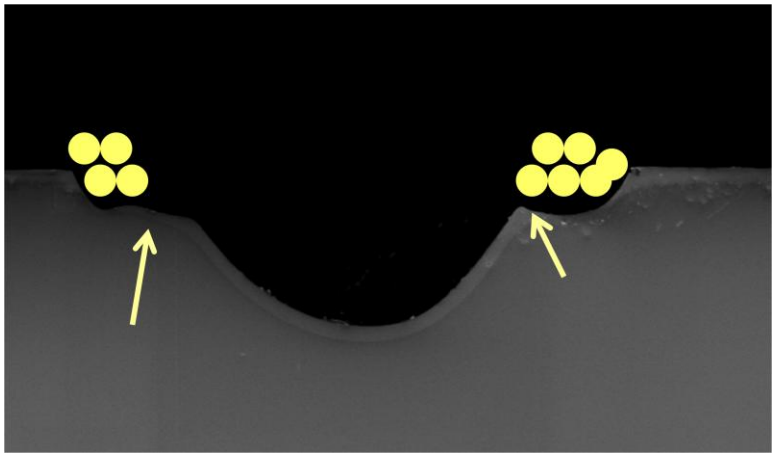


(b)

Figure 5.3: SEM image of a local BSF formation using etching paste for via patterning (a) Good BSF from a good cell (b) Bad BSF from shunted cell

As this cell structure moves towards higher efficiencies and manufacturability, alternate means of rear via definition would offer better flexibility and robustness to the process. This provided the motivation to explore laser opening of the vias. Various laser options are compared in this chapter and an optimal choice is identified.

5.3 Identification of Laser Options

Four different lasers were tested as possible candidates for ablation of vias in different modes to arrive at the choice of an optimal laser wavelength and mode of operation. The details are provided in Table 5.1.

Table 5.1: A summary of the laser systems employed for ablation in this work

Type	Wavelength	Mode
UV Laser- Nanosecond	355 nm	Pulsed
CO_2 Laser	10600 nm	CW
Fiber Laser - IR	1064 nm	Pulsed
Green Laser	532 nm	Pulsed

5.4 Dielectric Ablation using a Nanosecond UV Laser

An Avia 355 laser with nanosecond pulsewidth was one of the choices for laser ablation of rear dielectrics. An earlier study [69, 70] identified the UV laser (355 nm) as a candidate that produces minimal surface damage with minimal absorption by the silicon

substrate. This particular laser had a gaussian beam profile and the incident power per pulse could be modulated by varying the pulse repetition frequency, as seen in figure 5.4. This relation was used to optimize the power to obtain complete ablation of the rear dielectric, which was verified using optical microscopy imaging and 3D confocal microscopy. Based on this characterization, it was observed that for the specific rear dielectric stack used in this study, a pulse power of ~200 µJ at ~55 kHz resulted in optimal via definition with minimal damage to the surrounding dielectric (figure 5.5). After this optimization, the laser was used in cell fabrication for comparison with those fabricated by screen printing an etching paste.

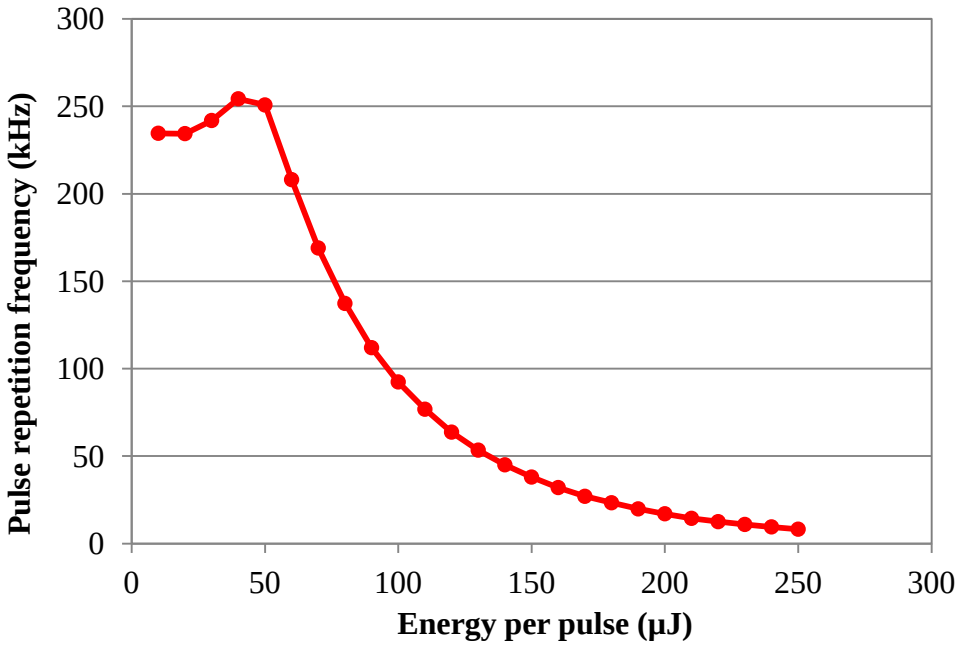


Figure 5.4: Relation between pulse repetition frequency and energy per pulse of the UV Laser

5.4.1 Experimental details of Cell Fabrication with Dielectric Ablation using UV Laser

Delta-STAR cells with etching paste as well as laser ablation were fabricated exactly the same way before and after the definition of vias. The 75 Ω/□ passivated emitter and dielectric passivated rear surface were obtained in a single high temperature step. A screen-printing paste (from Merck KGAA) was used for the definition of vias through the rear dielectric on the standard Delta-STAR cells. Front Ag and rear Al contacts were screen printed and co-fired. A modified cell isolation technique involving dicing and chemical etching of nine 4 cm^2 cells on 100 mm diameter wafers was employed followed by a forming gas anneal.

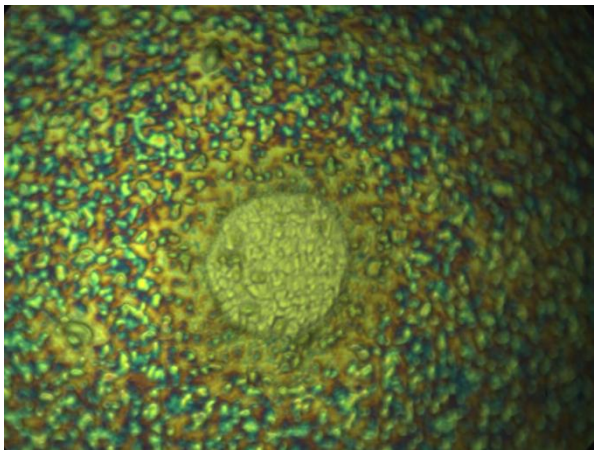
Vias were ablated through the rear dielectric stack to obtain a pattern identical to that obtained by the etching paste. Two different rear patterns were defined using the laser, while keeping the area fraction of vias identical. Multiple pulses of the laser were used to open vias that were identical in size and pitch to the screen printed vias, ~100 µm vias spaced 800 µm apart. In order to make the pattern simpler and to increase throughput, vias were also defined by a single pulse with a different via size and appropriately modified pitch in order to maintain the average area fraction of vias. This resulted in a rear pattern with vias of 53 µm diameter spaced 435 µm apart. Cell performance from this preliminary experiment was compared with measurement of I-V characteristics supported by cell characterization through IQE and reflectance measurements. Analysis of the silicon surface at the vias and the local back surface field formed under the contact was performed using optical and scanning electron microscopy.

5.4.2 Imaging and Analysis of vias defined using etching paste and UV laser

The effect of the laser ablation on the surface of the silicon and the selectivity of the process was analyzed using a microscope. While attempts were made to improve selectivity of the ablation through optimization, it was not completely eliminated and there was some damage to the silicon surface. Preliminary analysis of the surface damage was done by observing the vias under an optical microscope. The correct balance of energy per pulse is sought to remove the dielectric completely while introducing minimal damage to the silicon surface and subsurface bulk. The resulting images are shown in figures 5.5(a)-(c). Surface roughness is high in vias formed by the UV laser, which also results in a material accumulation around the edge of the vias. However dielectric ablation within the via appears to be complete with the power setting used in this study.

The quality of the BSF is closely related to the quality of the vias and hence can have a significant effect on the cell performance. The quality of BSF obtained on cells fabricated using the UV Laser was analyzed. This was compared to the BSF obtained on wafers using the screen printed etching paste. The cross section of a point contact was observed under an SEM after cleaving the sample. A difference in contrast can be seen between the bulk Si and the BSF around the contact metal. This band, as seen in figures 5.6(a)-(c), is continuous around the contact but varies in thickness. The formation of a thick and continuous BSF is critical for high efficiency LBSF cells, particularly to isolate the metal contact from the surrounding areas which are dielectric passivated. It was observed that ~5-6 μm thick BSF was present around the contact in both types of vias. The thickness and uniformity of the BSF formed in vias using multi-pulse laser ablation was also

similar to the ones formed in vias using single-pulse ablation. The BSF was found to be thickest in the middle and tapered closer to the edges. It was thinnest near the surface of the silicon. While the BSF was thin in certain areas, its existence around the entire contact, which is critical to the performance of this cell structure, was proven. It was also observed that the shape of the local contact and BSF was identical in both cases indicating that the contact formation and alloying to form the BSF was not affected by the surface morphology. Thus, a small amount of surface damage by the UV laser can be tolerated for this particular cell structure.



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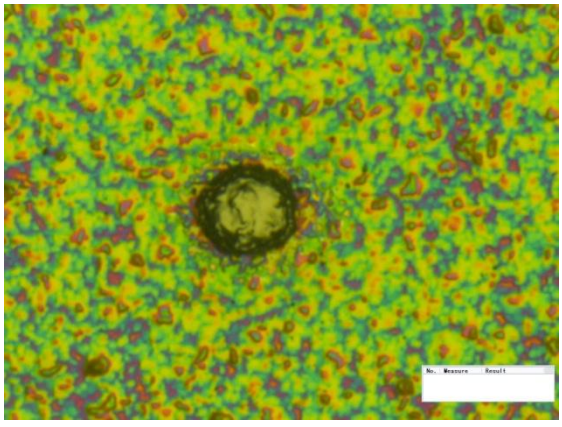

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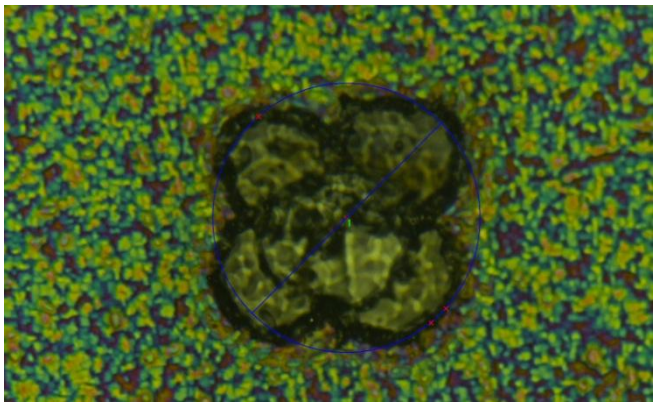


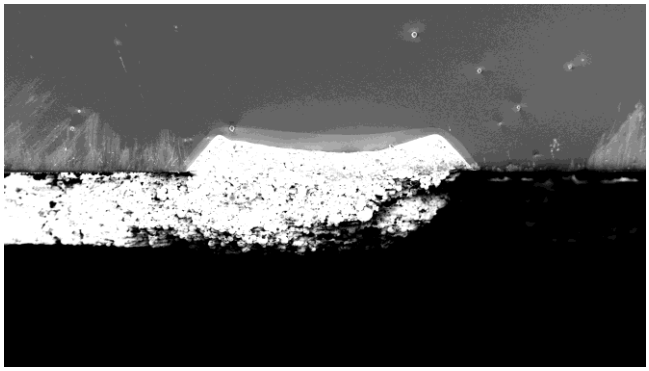
(c)

Figure 5.5: Optical microscope Image of typical via defined using (a)etching paste (b) UV laser (1 pulse) (c) UV laser (5 Pulses)

5.4.3 Results and Discussion of Cell Results and LBSF Formation

The aforementioned Delta-STAR process was used to fabricate nine 4-cm^2 cells on 100 mm diameter, 300 μm thick FZ silicon wafers which had a base resistivity of 1.3 Ω.cm. The best cell fabricated using etch paste for definition of vias resulted in a peak efficiency of 20.3%. The best efficiency obtained using laser ablation of the rear dielectric was 20.0% with the 5 pulse via and 20.1% with the single pulse via. The cell V_{OC} and J_{SC} were comparable for all three types of vias. Cells with the multi pulse method of via definition had the highest cell V_{OC} and J_{SC} but had a slightly lower FF resulting in a similar overall efficiency. These cell parameters are also comparable to the previous best Delta-STAR cell reported on a 2.3 Ω.cm wafer and can be seen in Table 5.2. Preliminary modeling shows that due to the difference in base resistivity, the higher FF compensates for a slightly lower J_{SC}, resulting in an identical efficiency. Overall these voltages and currents represent a significant improvement over full Al BSF cell

structures. This cell is the highest efficiency cell fabricated using laser ablation of vias, proving the feasibility of use of the UV laser for selective removal of the rear dielectric.



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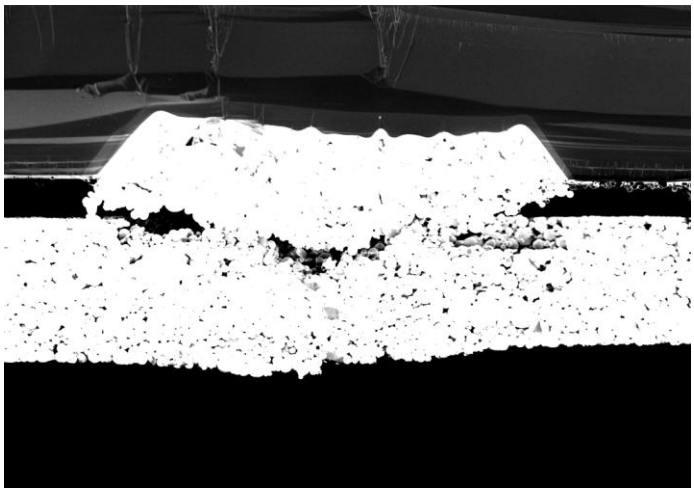

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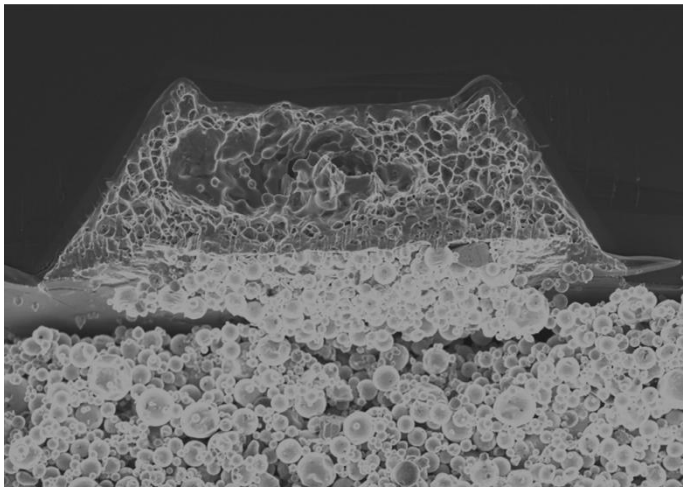


(c)

Figure 5.6: SEM image of contact and BSF obtained using (a) screen printed etching paste (b) ablation with UV Laser (5 Pulses) (c) ablation with UV Laser (1 Pulse)

Table 5.2: Summary of data from cell measurement

Cell	Resistivity (ohm.cm)	Voc (V)	Jsc (mA/cm^2)	Efficiency (%)	Fill Factor (%)
Screen printed paste	1.3	0.657	38.7	20.3	79.8
Laser ablated – 1 Pulse*	1.3	0.652	39.0	20.1	79.0
Laser ablated - 5 Pulse	1.3	0.653	38.6	20.0	79.5
Screen printed paste*	2.3	0.653	39.4	20.1	78.1

*- Measured at NREL with 3.8 cm^2 aperture

5.4.4 Characterization and Modeling of 20% Efficient UV Laser Ablated Cells

In order to compare the effect of the laser ablation of the rear surface, the cells were characterized by measuring their reflectance and Internal Quantum Efficiency (IQE). Data was collected for wavelengths in the range of 300 – 1200 nm at 10 nm intervals. All cells had a similar emitter with a sheet resistance of ~75 Ω/□ passivated identically. The rear surface was passivated with an identical dielectric-metal stack, so the only variation was the method of defining rear vias. The IQE response of these cells at wavelengths between 900 and 1100 nm is more relevant for the study of rear passivation. A comparison of the measured IQE from the representative cells of each case can be seen in figure 5.7. As a reference, the measured IQE of the previously reported 20.1% efficient cell is also provided. It can be seen that the cells with vias defined by screen printed etching paste had the best long wavelength response suggesting that the absence of via surface damage may result in slightly better passivation of the rear surface. Cells ablated with the UV laser with a single pulse and 5 pulses have very similar response, but are slightly inferior to that of the etched vias. However the overall quality of the rear passivation is similar and comparable. PC1D modeling was used to fit parameters to these measured curves. The best cell (20.3%) formed with etching paste showed a modeled BSRV of 125 cm/s. This was obtained by matching the long wavelength with PC1D, and using an assumed bulk lifetime of 1.2 ms. As seen in the figure, the rear response of these other cells can be modeled with a slightly higher BSRV of ~150 cm/s. This slight change in BSRV is still within the limits of process and measurement variations and doesn't affect the cell performance adversely, as seen from the cell IV data (Table 5.2). This provides further evidence that the observed slight damage due to the

laser on the surface is not critical to the cell performance as it may be consumed by the formation of the local BSF. The final quality of the BSF and its uniformity is more important to the passivation and elimination of parasitic shunts. Figure 4 indicates that the variations in measured J_{SC} of the best cells in Table 5.2 may be related to the slight difference in the anti-reflection coating and reflectance.

It is noteworthy that identical cell efficiencies were obtained with two different rear via geometries. This increased the throughput of laser ablation by nearly a factor of 5, which is a significant contribution. The high cell efficiency obtained using smaller vias of ~53 µm also confirms that the performance of real Al paste is not restricted by the size of the rear feature. This observation is important when considering that certain pastes are limited by their viscosity and can result in non-optimal performance with small feature sizes [95].

This research also investigated the effect of via spacing on parasitic shunting. In an earlier study on PERF-type cells [29], it was concluded that cell efficiency varied with the rear contact pitch when the rear surface was passivated with a floating junction. As rear contact pitch increases, the potential difference between contacts decreases, thereby reducing the parasitic current flowing between the rear contact metal and the floating junction. This results in higher cell efficiency. As discussed in chapter 2, field effect passivation exhibits characteristics that are very similar to floating junction passivation. However in these experiments, it is observed that a change in the rear contact pitch does not alter the cell performance and the overall cell results are only affected by the rear metal fraction. This leads to the conclusion that while the rear surface may be inverted by

the high, positive, fixed charge in the dielectric stack, the local BSF creates sufficient isolation between the contact and the inversion layer to prevent parasitic losses. This observation suggests that this high efficiency is independent of rear contact geometry and can be modified based on substrate resistivities without parasitic losses

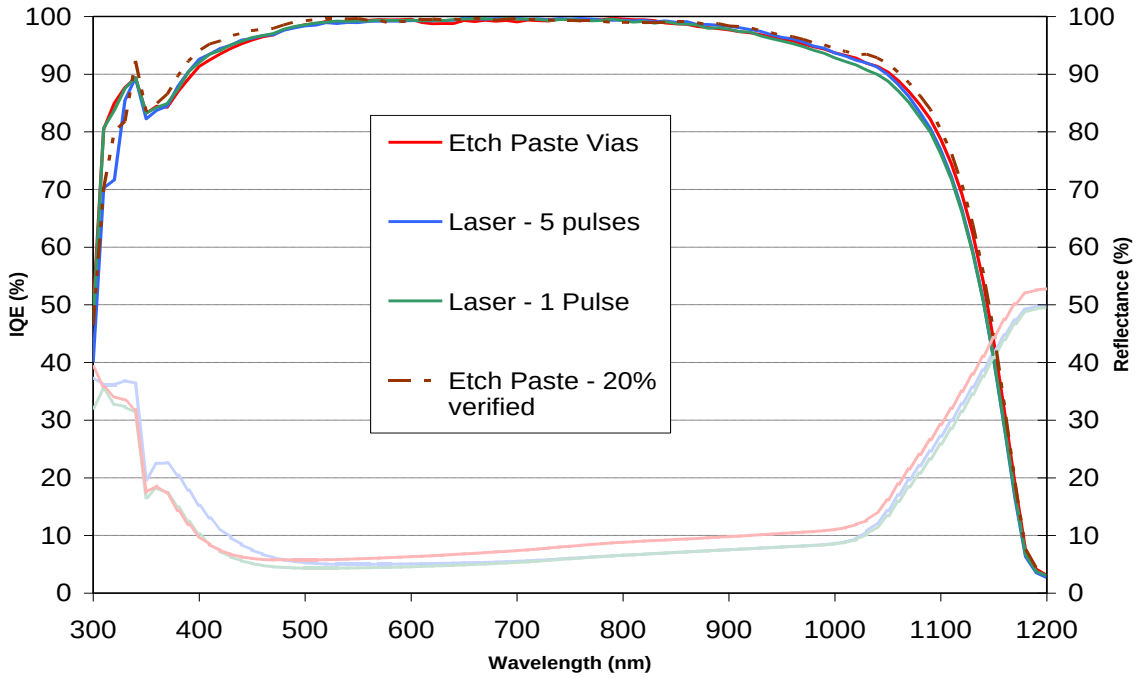


Figure 5.7: Comparison of long wavelength IQE response of typical cells

5.5 Dielectric Ablation using Carbon Dioxide Laser

After establishing the success of the UV laser in achieving 20% cells, three different lasers were examined for use in the Delta-STAR technology. The first new candidate was the CO_2 laser with a wavelength of 10.6 um. It was used in the continuous wave mode and vias of the appropriate dimension were obtained by movement of the laser focus spot within each via. Initial ablations were performed on samples with a dielectric stack identical to cell wafers. Optimization of power settings were performed to ablate all the

dielectric and reveal the Si underneath in the vias. Care was taken to replicate the geometry from the screen-printed high efficiency cells mentioned in the earlier section. Initial observations under the optical microscope revealed extensive damage to the silicon surface that appeared to be because of melting and resolidifiction. SEM observation of these vias also revealed that this resolidification resulted in subsurface cracks under the via region. Since the wavelength of the CO_2 laser is not absorbed in the silicon bulk, at the initial power settings, the laser absorption was found to have an effect on the front SiN_x and possibly the emitter underneath.

As part of the initial experiment, local BSF cells were fabricated using CO_2 laser ablation at this initial power setting. All other processes in the fabrication of these cells were identical to the high-efficiency Delta STAR. The cells produced a peak efficiency of 19.0% with an average of 18.7%. A brief summary of these results can be seen in table 5.3. While cell V_{OC} was slightly less than the V_{OC} measured on the best Delta-STAR cell fabricated using a UV Laser (table 5.2), the biggest loss in cell performance was due to the low J_{SC}. Fill factor was also slightly lower compared to conventional Delta-STAR cells. Some of these losses were attributed to the non-ideal ablation characteristics of the laser at this power setting.

Table 5.3: Summary of results of IV testing of CO_2 laser ablated sample

Cell ID	Voc (mV)	Jsc (mA/cm^2)	Eff (%)	FF (%)
Best Cell	650	37.5	19.0	78.0
Average	648	37.3	18.7	77.2

5.5.1 Optimization of Incident CO_2 Laser Power

CO_2 laser fluence was optimized to minimize side effects of the dielectric ablation. Five different power regimes were investigated by Laser spot size was maintained at 10-15 µm and, the laser was scanned within the via to completely ablate a via, 100×100 µm in size. The scan speed was also to alter the dwell time and fluence at each individual spot within the via. The different zones were numbered 1-5 as seen in figure 5.8 and the details of the settings are shown in Table 5.4. An optical microscope was used to obtain a top-down view of the ablated via and the exposed Si surface. Scanning electron microscopy was used to obtain a cross-sectional view of the silicon bulk around the via. The wafers were cleaved across vias to observe subsurface effects of the power and scan speed settings used in each zone. The results of these are seen in figures 5.9 – 5.13 below.

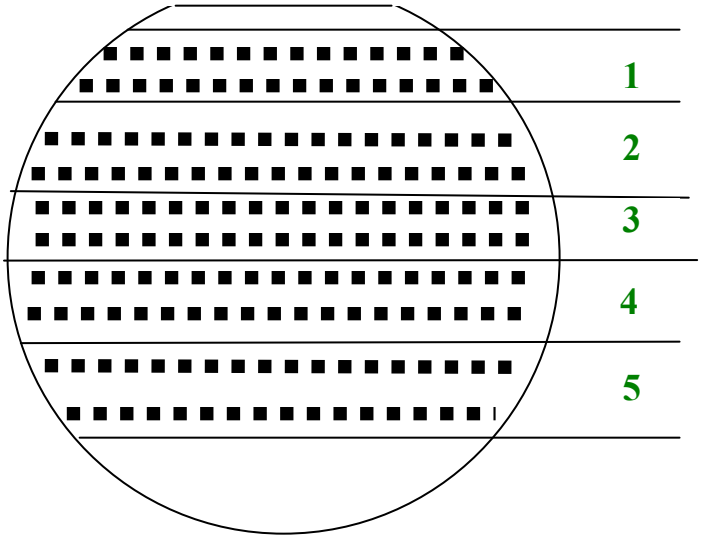


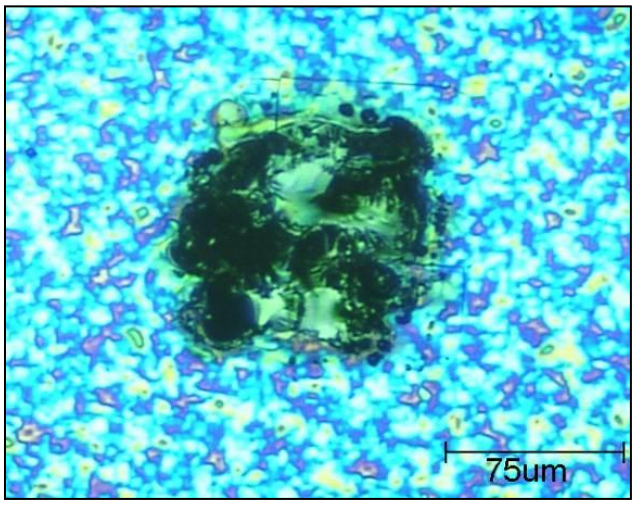
Figure 5.8: Schematic showing the different zones used for power optimization

Table 5.4: Power and scan speed settings used in each zone

Zone Number	Power Setting	Scan speed
1	High	High
2	High	Medium
3	Medium	Medium
4	Medium	Low
5	Low	Low

Optical microscope images (figures 5.9 - 5.13) revealed that settings used in zone 1 and zone 2 caused significant damage to the surface of silicon within the ablated via. SEM images showed that subsurface melting was also very high in these cases resulting in pieces of re-solidified Si breaking away from the bulk within each via. It should be noted that Si pieces could have been dislodged as a result of cleaving the Si wafer prior to observation. However this behavior was not observed when cleaving Si wafers etched by the screen printed paste and hence, was considered an effect of the high power settings. It was also observed that lower power settings resulted in fewer and smaller dislodged pieces of silicon compared to those in zone 1 and 2. Appearance of subsurface cracks in the silicon bulk would adversely affect the cell performance. Re-solidified silicon was also an undesired side effect of laser ablation as it created a new interface in the silicon bulk and would lead to increased recombination and an overall loss of cell efficiency. If the re-solidified silicon region is minimal, then it would get consumed during the subsequent formation of a BSF during contact firing and hence, not create the new interface in the silicon bulk.

Upon inspection of vias in zone 5, it was noted that surface damage and subsurface cracks were minimal. However, the ablation of the dielectric was incomplete due to low power. Based on these results, optimized power and scan speed combination was used in zones 3 and 4 and for actual cell fabrication.



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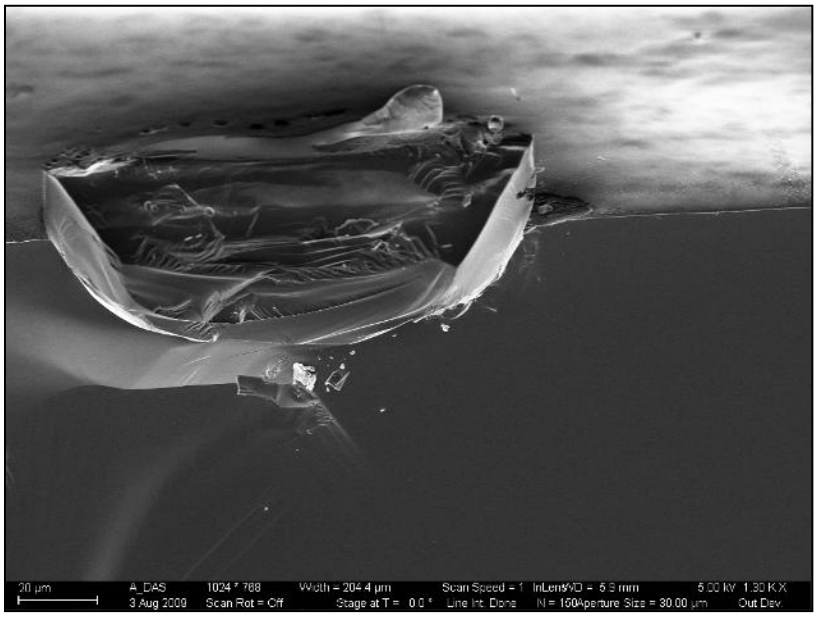
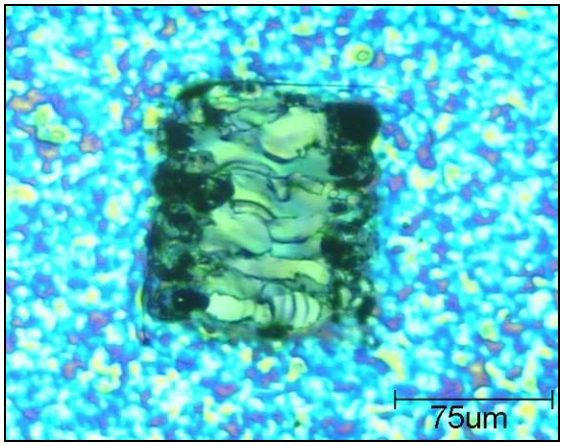


(b)

Figure 5.9: Images of via ablated in zone 1 (a) Optical microscope (b) SEM



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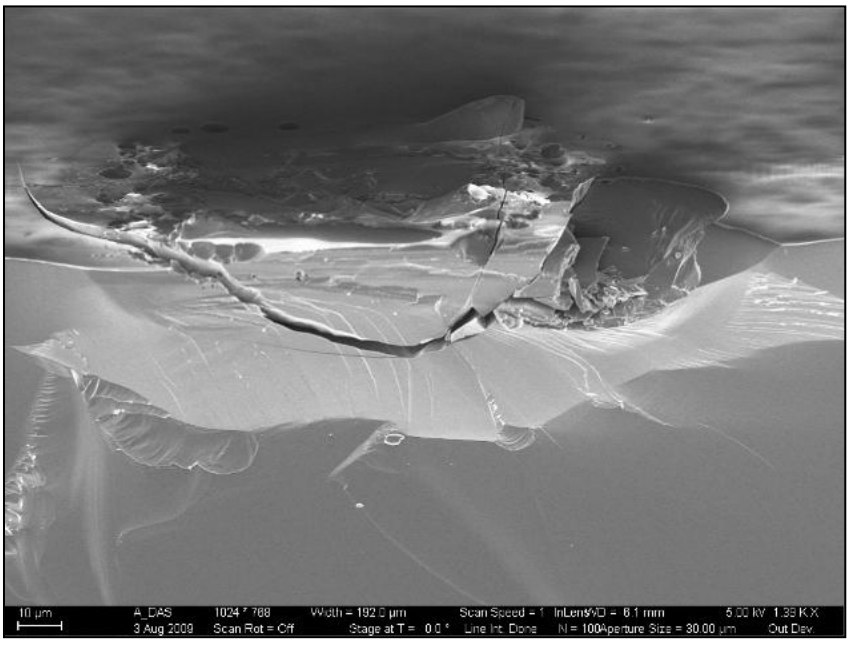

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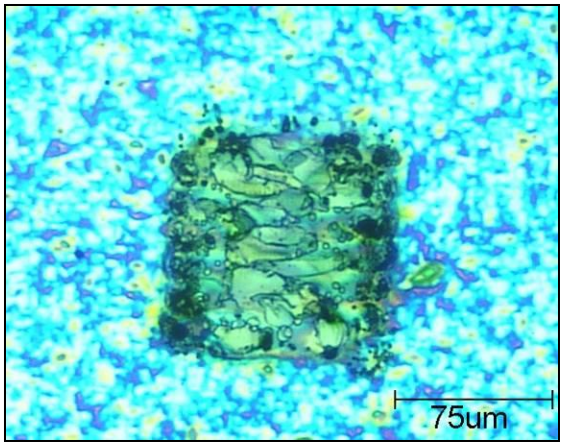
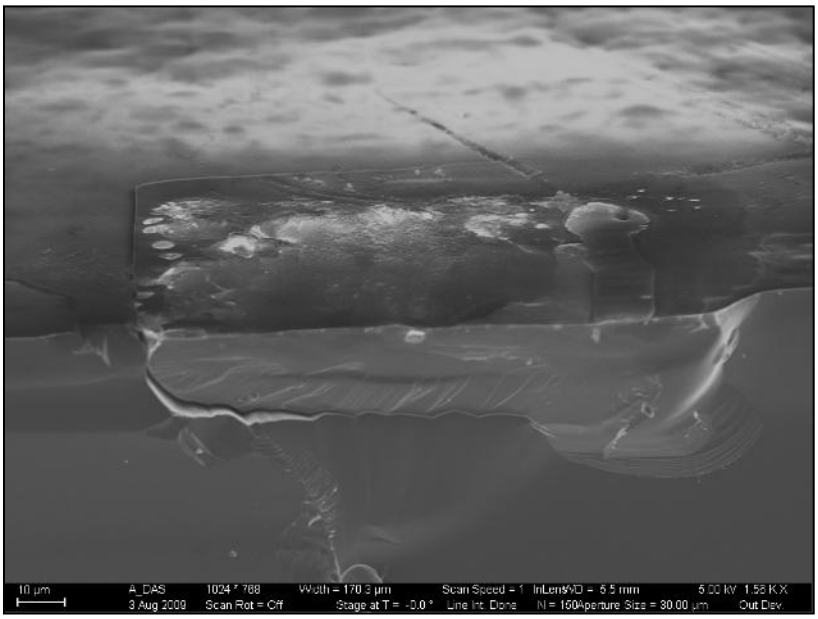
Figure 5.10: Images of via ablated in zone 2 (a) Optical microscope (b) SEM

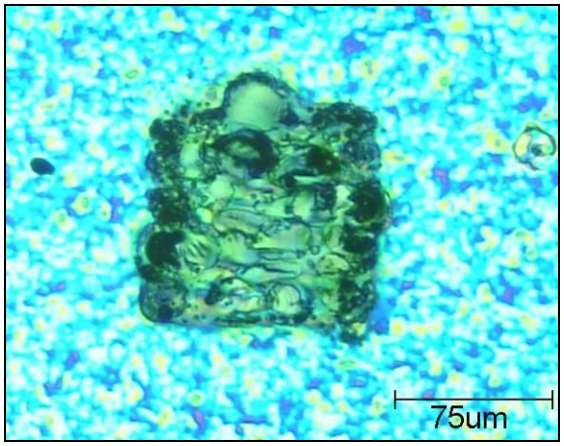


(a)

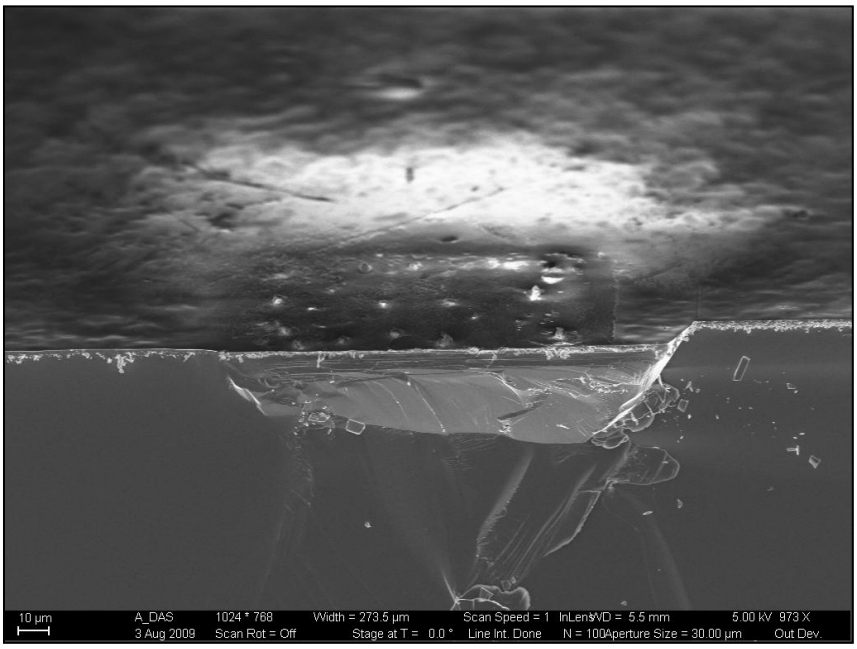


(b)

Figure 5.11: Images of via ablated in zone 3 (a) Optical microscope (b) SEM

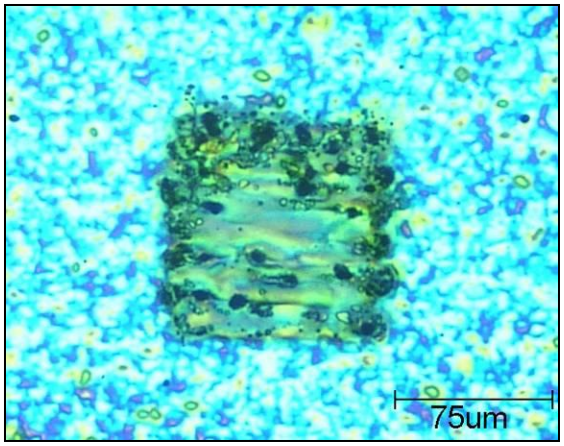


(a)

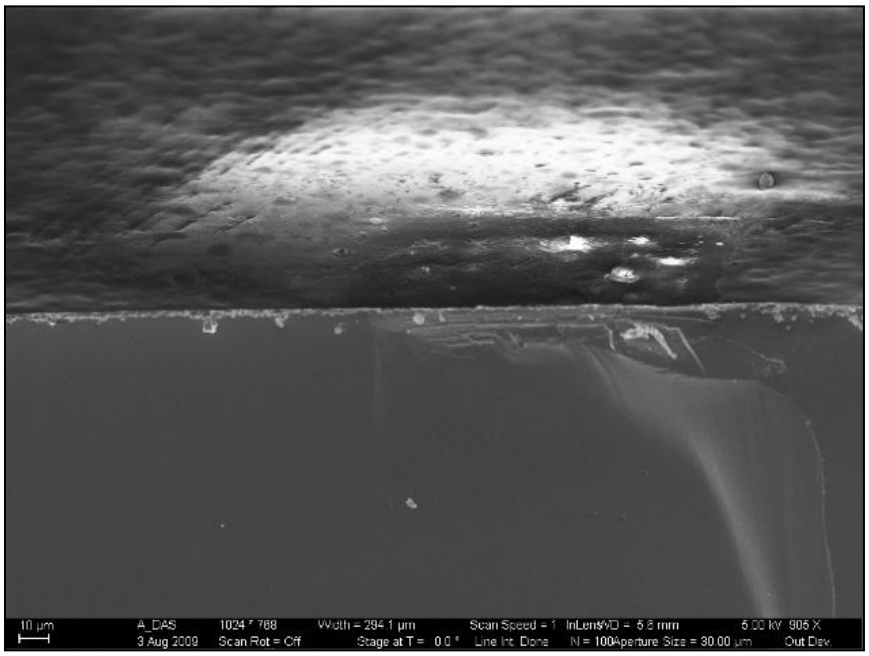


(b)

Figure 5.12: Images of via ablated in zone 4 (a) Optical microscope (b) SEM



(a)



(b)

Figure 5.13: Images of via ablated in zone 5 (a) Optical microscope (b) SEM

5.5.2 Cell fabrication after Ablation with Optimized Laser Power

Power and velocity settings from zones 3 and 4 were used to ablate 2 wafers each. Two different geometries were used for cell fabrication – the standard geometry of 100 µm vias with 800 µm spacing and a second pattern with 75 µm vias and 600 µm spacing. The total metal fraction was kept the same to ensure similar passivation quality without the series resistance losses between rear contacts. During screen printing of contacts, all wafers broke into multiple pieces, as seen in figure 5.14. This breakage of wafers was not typical and occurred only on samples ablated with the CO_2 laser. This breakage was attributed to residual stresses caused by the melting and resolidification of the silicon in vias during laser ablation. Melting and resolidification was minimized with optimized power settings, but could not be completely eliminated.

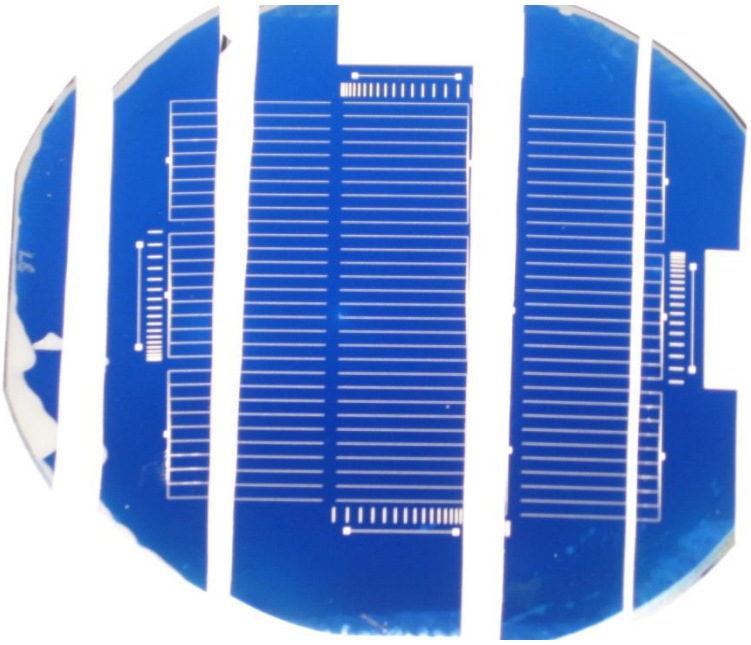


Figure 5.14: Wafer breakage during screen printing

Only 6 cells on 1 wafer survived. The best cell produced a peak efficiency of 20.2% with a cell with a high V_{OC} and J_{SC}. These voltages and currents were slightly different from the Delta-STAR cells fabricated using the etching paste because of the lower substrate resistivity. The 6 cells also had fairly uniform performance resulting in an average of 20.0% as seen in table 5.5. This improved performance was observed on wafers with the modified rear pattern of 75 µm vias spaced 600 µm apart. The best cell was characterized by measuring the spectral response and reflectance and calculating the IQE from these. When compared to the best conventional Delta-STAR cell, the response was found to be very similar overall with only a slightly inferior BSRV (Figure 5.15). BSRV for this laser ablated cell was ~200 cm/s compared to 125 cm/s for the conventional Delta-STAR cell. Thus the regions where stresses did not cause wafer breakage, local BSF formation maintained rear passivation to produce high cell efficiency.

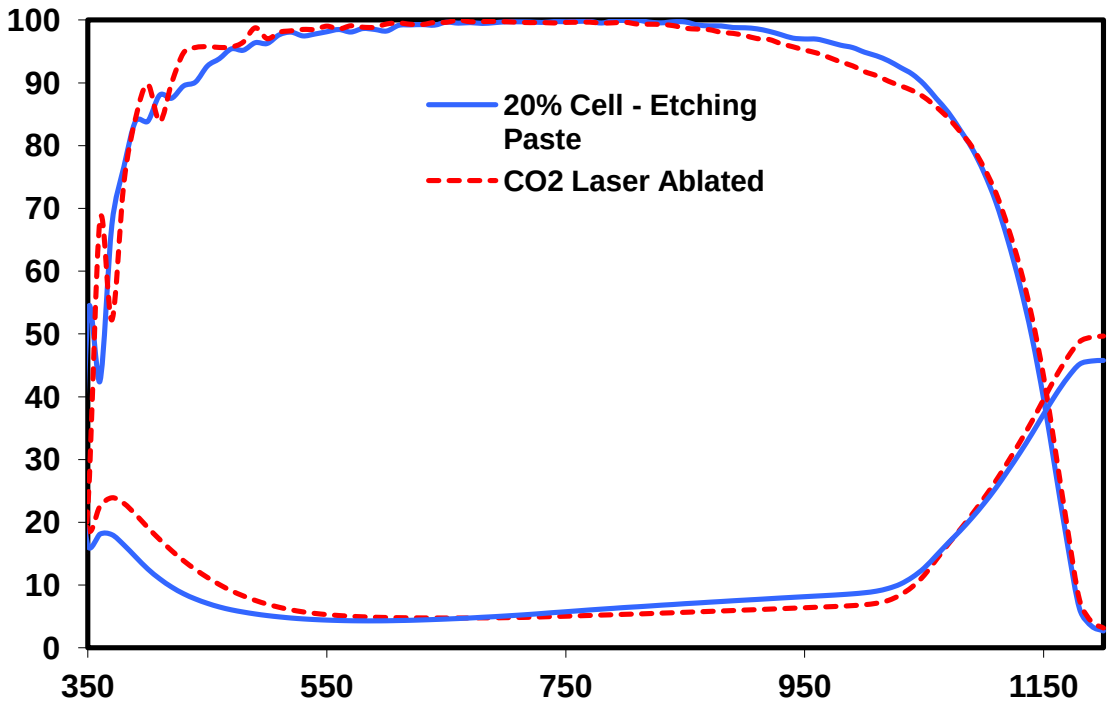


Figure 5.15: IQE comparison of best cells fabricated using CO2 laser and conventional via etching

Table 5.5: Summary of results of IV testing of CO_2 laser ablated sample with optimized power settings

Cell Name	Voc (mV)	Jsc (mA/cm²)	Eff (%)	FF (%)
Best cell	663	38.6	20.2	79.0
Average	662	38.6	20.0	78.4

To confirm that CO_2 laser ablation caused stress in the silicon wafers, samples with and without laser ablation were subjected to three point bending stress test. 13 laser ablated samples and 8 non-ablated silicon samples were examined. It was found that the laser ablated samples were weaker by a factor of 2.8 – 128 MPa bending stress compared to

362 Mpa bending stress for non-ablated samples, respectively. The latter strength is comparable to normal unprocessed silicon substrates. These results clearly indicate that CO_2 laser ablation in the continuous wave mode results in side-effects in the bulk silicon that render this method not feasible for large scale production of local BSF devices.

5.6 Preliminary Study of Dielectric Ablation using Green Laser

Some studies have reported [69, 70] that green lasers with nanosecond pulsewidths display selectivity of ablation comparable to UV lasers. A green laser (Nd-Yag) of picoseconds pulsewidth was used for preliminary experiments. Initial optimization of power settings was performed on a dielectric stack and optical microscope imaging was used to achieve complete ablation of dielectric. The Gaussian profile was converted to a top-hat profile using beam shaping. A top-hat profile is more suited for opening vias through the rear dielectric because of its abrupt energy profile. This profile leads to a uniform characteristics within a via with minimal damage to the surrounding dielectric as seen in figure 5.16. Since the via is defined better when compared to a Gaussian beam profile, the actual via dimensions match closely with the designed pattern. A via size of 40 µm was obtained with a single pulse. The rear contact geometry was optimized to maintain a rear metal fraction (~1.25%) similar to that of the conventional Delta-STAR cells made with a screen printed etching paste. This was achieved by reducing the rear contact pitch from 800 µm to ~320 µm.

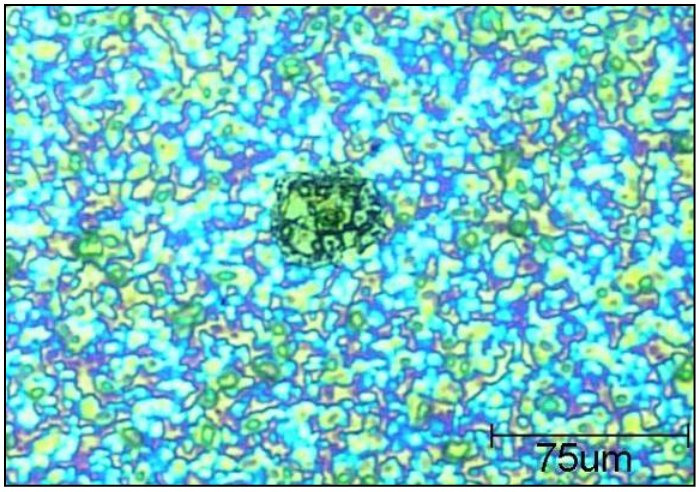


Figure 5.16: Optical microscope image of a via ablated using a green laser

5.6.1 Fabrication of Cells with Dielectric Ablation using Green Laser

Delta-STAR cells were fabricated on FZ wafers. Table 5.6 shows that a peak efficiency of 20.0% was achieved with cell parameters comparable to the best Delta-STAR cell (Table 5.2). Average efficiency of 9 cells on one wafer was 19.7%. Characterization of the best cell using IQE also showed that the response of this cell was comparable to cells fabricated using the UV laser and screen printed etching pastes. The long wavelength response was observed to be slightly inferior but well within the margins of process and measurement variations.

Table 5.6: Summary of I-V results on wafer ablated using a green laser

Cell Name	Voc (mV)	Jsc (mA/cm^2)	Eff(%)	FF (%)
Best Cell	650	39.1	20.0	78.8
Average	651	38.8	19.7	78.1

Since the use of smaller vias and a decreased pitch produced similar results to the original screen printed geometry, it proves that this rear contact design can be modified without being limited by the Al paste or rear parasitic losses. Since throughput of the green laser with picoseconds pulsewidth was slightly higher than the UV laser, it could be more suitable for large scale production.

5.7 Laser ablation using Fiber laser

Finally, fiber laser was evaltuated as a fourth candidate for opening vias through dielectric for making Delta-STAR cells. The availability of a continuous wave fiber laser (1064 nm) prompted a feasibility study in this thesis. Similar to the CO_2 laser, the spot size of the fiber laser was 10-15 µm wide and required scanning to open ~100 µm wide square vias. As before, laser power and scan speed were optimized. Vias were examined using an optical microscope to ensure complete ablation of the dielectric. The ablated vias were found to have significant roughness compared to the other laser ablated vias. The optical microscope image appears dark and the stripes from the laser scans can be distinctly seen in figure 5.17. This indicates high absorption of energy by the silicon surface, resulting in significant redistribution of silicon by melting and solidification. These observations were validated using SEM imaging (figure 5.18). Vias ablated using the fiber laser were extremely non-uniform. At low magnification, it was observed that the scribed passes of the laser were discontinuous within vias. At higher magnification, it was evident that there were large areas within vias where the dielectric was not ablated, leaving regions of dielectric in between stripes of ablated Si. In addtion, the surface

damage indicates a molten Si and solidification front as the laser scanned the via. This accounted for the dark surface observed using the optical microscope. In addition, the incomplete ablation of dielectric within the via could result in a non-uniform BSF.

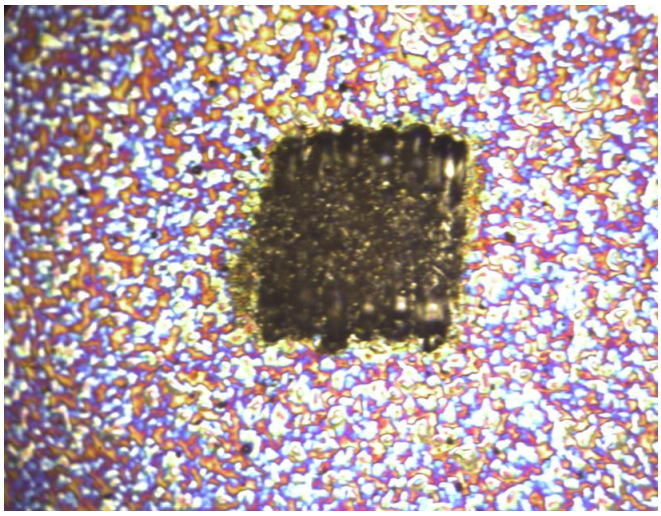


Figure 5.17: Optical microscope image of a typical via ablated using a fiber laser

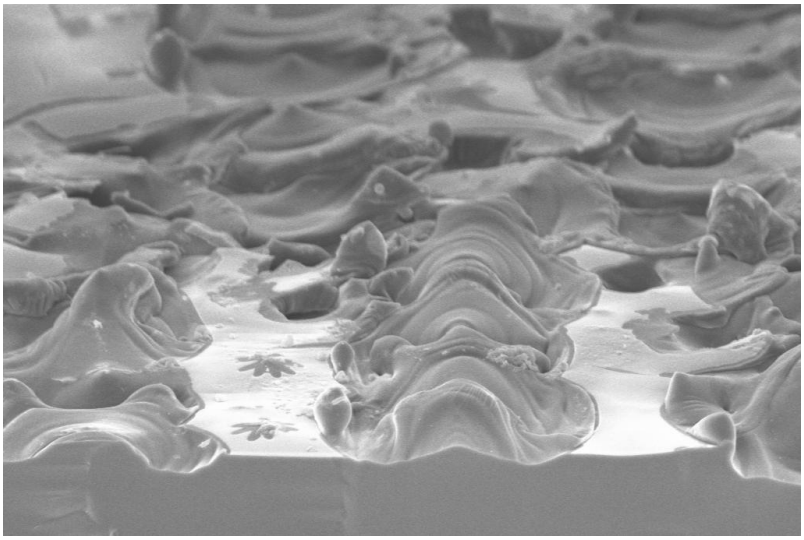


Figure 5.18: High magnification SEM image of a typical via ablated using a fiber laser

Again Delta-STAR cells were fabricated on FZ substrates using the fiber laser for dielectric ablation. The peak efficiency was 19.9% with cell parameters comparable to vias defined by screen printing. The overall uniformity of cell performance was also fairly uniform. It was surprising that even with so much non-uniformity in the silicon vias did not adversely affect cell performance. It is possible that the silicon damage is limited to the surface, so it gets consumed during the formation of a BSF, resulting in good rear passivation.

Table 5.7: Summary of I-V results on wafer ablated using a fiber laser

	Voc (mV)	Jsc (mA/cm^2)	Eff (%)	FF (%)
Best	653	38.7	19.9	78.6
Average	651	38.5	19.6	78.3

However, one of the disadvantages of this process was found to be the low throughput. Ablation of each 4" wafer using this fiber laser in a continuous wave mode involved processing times higher than 30 minutes. So, while the cell performance was found to be acceptable, this method was not investigated further as a candidate for use in large scale processing. From these experiments, it can be concluded that a fiber laser (1064 nm) may be compatible with LBSF technologies, if used in a pulsed mode, to improve process throughput.

5.8 Conclusion

High efficiency local BSF cells were fabricated using a UV laser for selective rear dielectric removal. The performance of the cells fabricated by UV laser ablation and screen-printed etching paste was very similar. Observation of the laser ablated vias under an optical microscope and SEM indicated that the vias formed using lasers had some amount of surface damage, but compensated by the formation of a good uniform BSF. Further cell characterization and analysis indicated that the overall quality of the rear passivation was maintained, which was also supported by SEM analysis and PC1D modeling. Laser ablation was found to provide a fast and reproducible alternative to the screen printed etching process. The replacement of the 5 pulse process by the 1-pulse process results in higher throughput while improving the quality of the vias and reducing chances of parasitic shunts. The flexibility offered can help optimize the rear contact design further resulting in an increase in efficiency beyond 20.5 % and provide a more commercially viable alternative for fabrication of high efficiency thin cells. Alternate lasers were considered for rear ablation. Carbon dioxide lasers were able to produce high efficiency but suffered from wafer breakage due to too much melting and solidification of Si in the vias. A fiber laser with 1064 nm wavelength also resulted in high efficiency when optimized, but suffers from low throughput. In general, lasers operated in the continuous wave mode are deemed unsuitable for this purpose. Some earlier studies have identified a green laser as an ideal candidate for various processes in solar cell fabrication. Preliminary results in this study identify the green laser as a viable candidate that can be used for future studies without loss in cell performance or throughput.

CHAPTER 6

APPLICATION OF DELTA-STAR TECHNOLOGY TO COMMERCIAL GRADE SUBSTRATES

6.1 Modeling the Impact of Thickness and Bulk Lifetime on LBSF Cell Performance

Previous chapters provided the foundation and development of laboratory scale high efficiency (20%) cells on thick FZ substrates using commercial-friendly screen printing and laser ablation technologies. In order to improve the manufacturability of this device design further, it needs to be fabricated on thin, large area, inexpensive substrates like thin Cz silicon. While there are cost benefits of moving towards Cz substrates, generally, the material quality is inferior to the float zone Si used in this study due to higher impurity content and oxygen concentration. PC1D model calculations were performed using inputs from the 20% efficient FZ cells varying the bulk lifetime. When the material is of a good quality, thicker substrates lead to a higher efficiency due to a higher absorption of the solar spectrum. Model calculations in figure 6.1 show that, it is beneficial to move towards thinner substrates with low bulk lifetimes. Since the bulk material is of a lower quality, use of thinner substrates reduces bulk recombination in the substrate and the full benefit of surface passivation can be harnessed. In addition, thinner substrates are also less sensitive to minor variations in bulk lifetimes. The cost of Si bulk material in solar cell production is a substantial portion of the overall cost (50-60%). So,

thinner substrates also help in reducing the production cost of solar cells. In addition, since LBSF cells do not suffer from warping of the wafer due to a much lower percentage of Al/Si contact area. However, there is a decrease in efficiency when fabricating cells on lower lifetime substrates. Besides, there are differences in surface quality, which could affect the quality of rear passivation. These factors are addressed in this section.

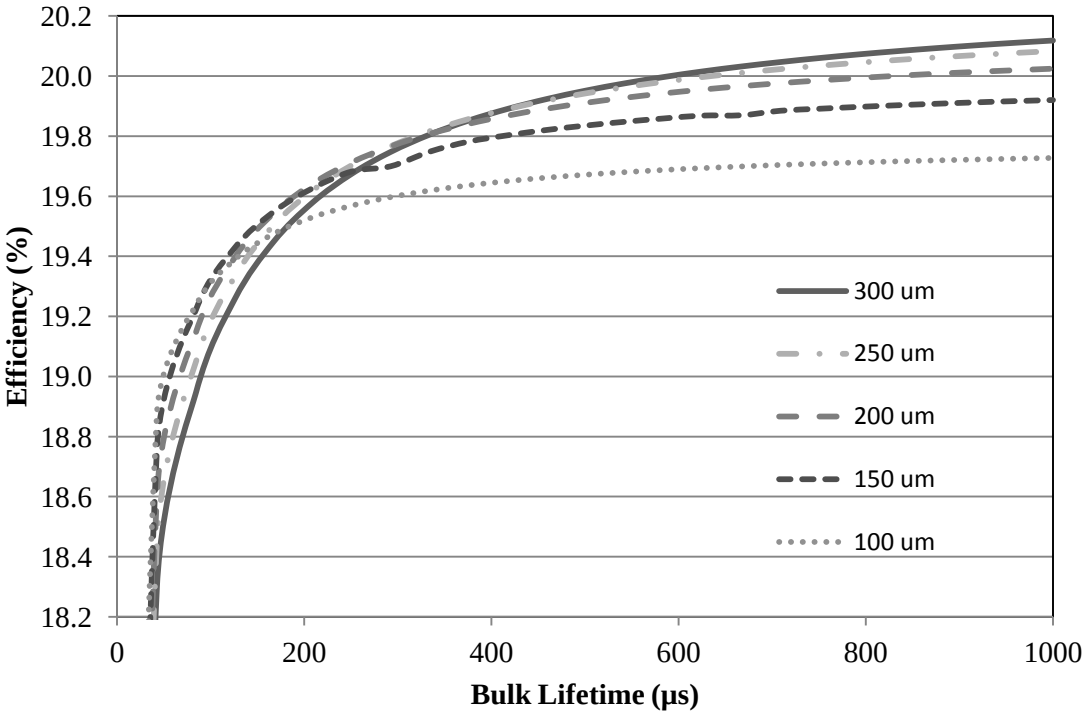


Figure 6.1: Results of PC1D simulation showing dependence of cell performance on substrate thickness and bulk lifetime

6.2 Understanding the Effects of Surface Finish on Passivation Quality

Local BSF cell technology that was studied and developed in this research relies on significant benefit from surface passivation, as outlined in the earlier chapters. The high

efficiency cells discussed earlier were fabricated on thick FZ substrates that had polished surfaces in the as-received form. As a result, the wafer surface did not contribute appreciably to the interface states (D_{it}) and the recombination at the interface was affected primarily by the quality of the dielectric growth. Therefore, when this local BSF technology is transferred to manufacturable thin substrates, the first factor to be examined is the quality of the rear surface and its impact on cell performance. Lower cost Cz and magnetically stabilized Cz (mCz) wafers were studied in this work by first subjecting them to alkaline surface treatments in KOH to remove saw damage and perform surface texturing. Typical planarization recipes were tested on FZ surfaces to optimize the surface condition for use with Cz substrates. Since treatment with KOH proceeds by an anisotropic etching of the silicon surface exposing only <111> surfaces, various recipes were compared to minimize surface roughness. Surface planarization was optimized with respect to time, temperature of the etching bath and concentration of the KOH solution, as each of these parameters affect the etching rate of silicon along different crystallographic axes. Surface planarization by new solutions and used solutions was attempted to optimize a recipe to achieve uniform surface results irrespective of age of solution. After planarization, the roughness of the rear surfaces was measured using an Atomic Force Microscope (AFM) scan. The resulting surfaces from different planarization processes were also imaged and analyzed by a confocal 3D microscope. Three of these surfaces and their respective surface roughness measurements can be seen in figures 6.2 – 6.4. The planarization recipe corresponding to figure 6.4 provided uniform results with used and new KOH solutions without significant waste of Si during the etching process.

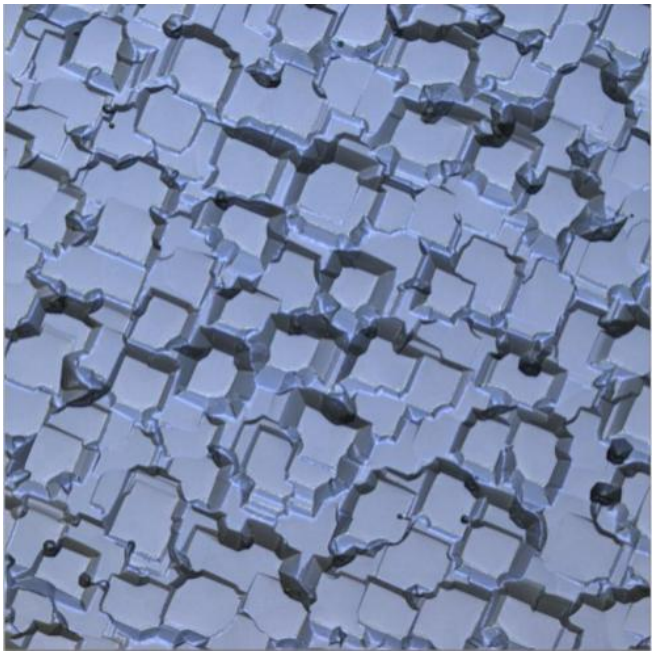


Figure 6.2: 3D Confocal microscope image of a planarized surface with RMS surface roughness of 1.31 µm

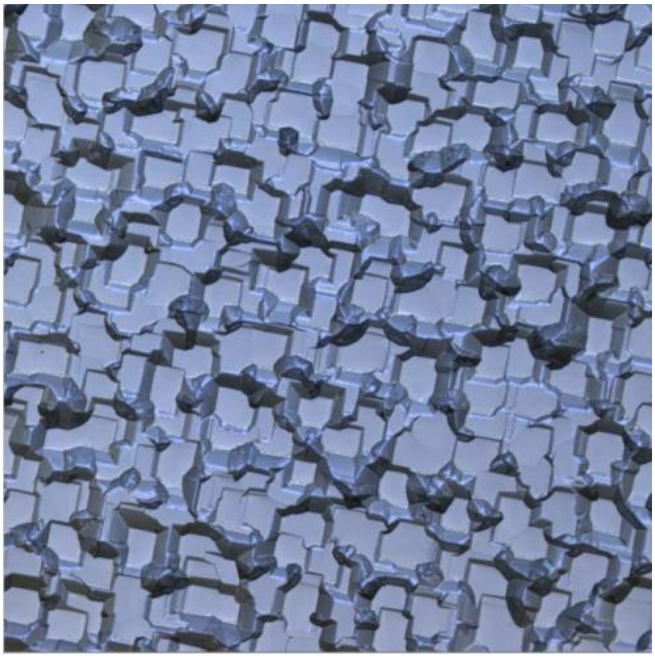


Figure 6.3: 3D Confocal microscope image of a planarized surface with RMS surface roughness of 1.46 µm

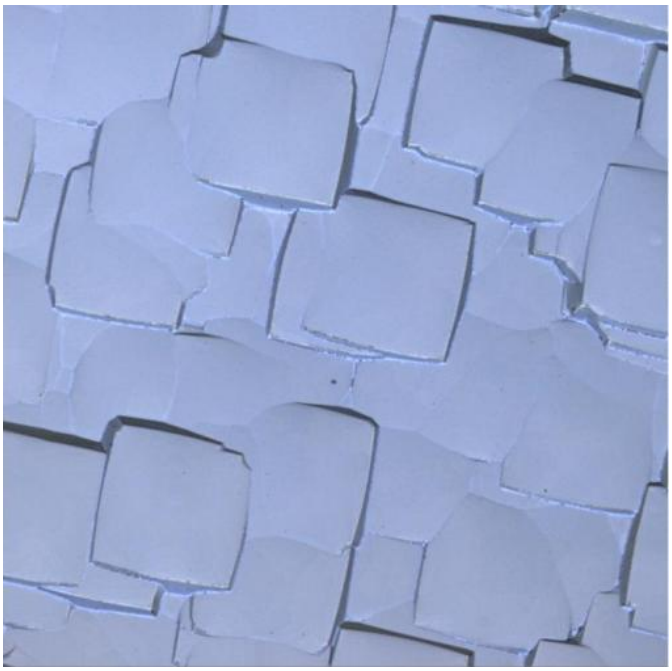


Figure 6.4: 3D Confocal microscope image of a planarized surface with RMS surface roughness of 0.75 µm

6.2.1 Effect of Surface Roughness on the Performance of Local BSF Cells

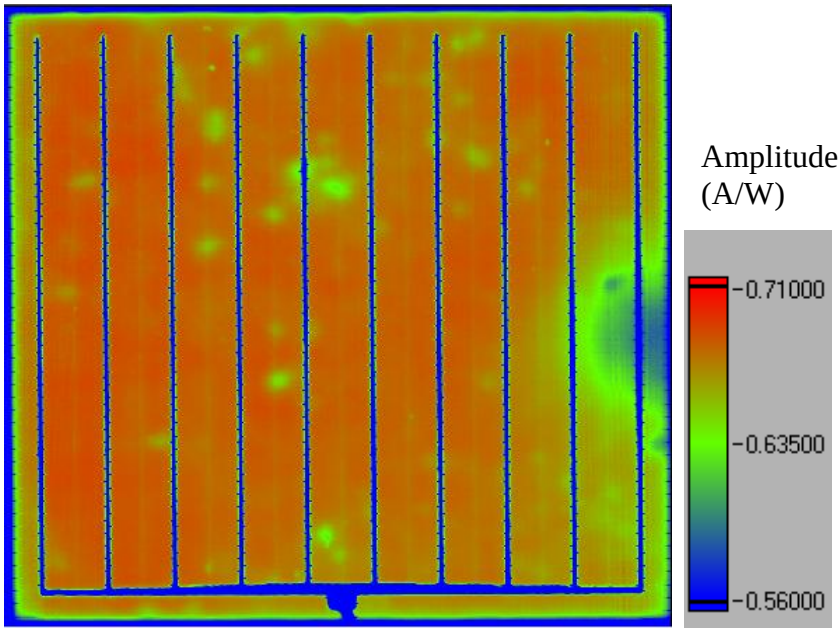
Cells were fabricated on wafers with different rear surfaces and their performance was compared to the measured roughness. As seen in Table 6.1, there was a good correlation between the measured roughness and cell V_{OC}. Since these cells were processed identically except for surface treatment, the variation in V_{OC} is related to the differences in rear passivation due to the surface roughness. Note that the lowest average roughness resulted in the highest cell V_{OC} indicating good planarization is critical for high efficiency advanced cells.

Table 6.1: Summary of results from surface roughness experiments on Delta-STAR cells

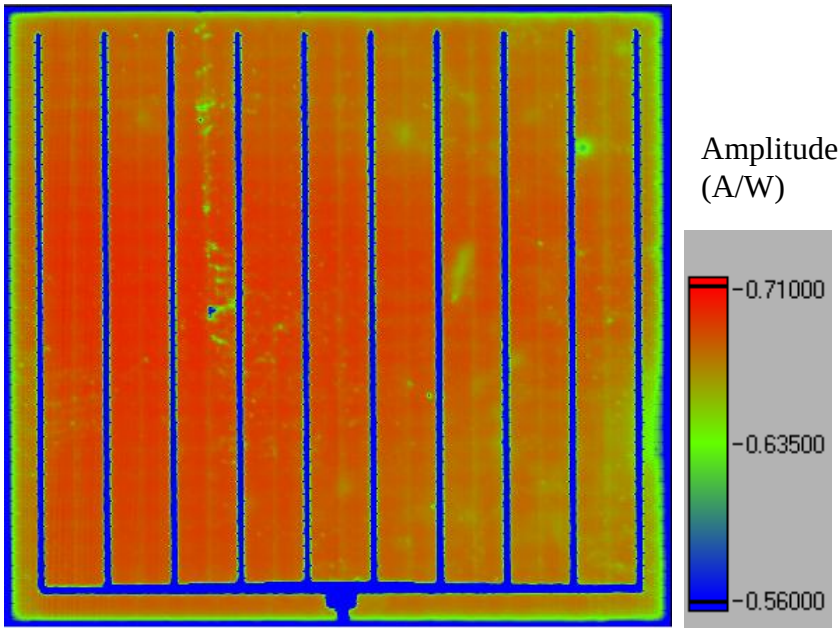
Wafer ID	KOH Concentration	Temp (deg C)	Time (min)	Average Voc (V)	Rq (nm)
1	17.7%	80	4	0.646	483
3	17.7%	65	18	0.657	156
4	9%	80	4	0.645	321
5	9%	65	6	0.643	202
6	9%	65	18	0.658	105.9
2 – As received	N/A	N/A	N/A	0.653	

To confirm this further, the best cell from each wafer was subjected to light beam induced current (LBIC) measurement using the PVSCAN 5000. This measurement, performed using a monochromatic laser beam of wavelength 980 nm, provides a map of the electrical response of the bulk and rear surface regions of solar cell [96]. LBIC response of three cells with KOH planarized rear surfaces with decreasing surface roughness are seen in figures 6.5 (a)-(c) and figure 6.5 (d) provides a reference LBIC response from a FZ wafer with a polished rear surface. It is clear that surfaces with a lower roughness produce a very uniform and high LBIC response, very similar to that of the reference surface. However as the roughness increases, LBIC response decreases and becomes more non-uniform, and in extreme case may lead to rear parasitic shunting (Fig 6.5a). This result is very important for the successful transfer of this local BSF technology to high efficiency large area substrates and indicates that rear side

planarization of large area commercial substrates is critical for high yield and performance.



(a)



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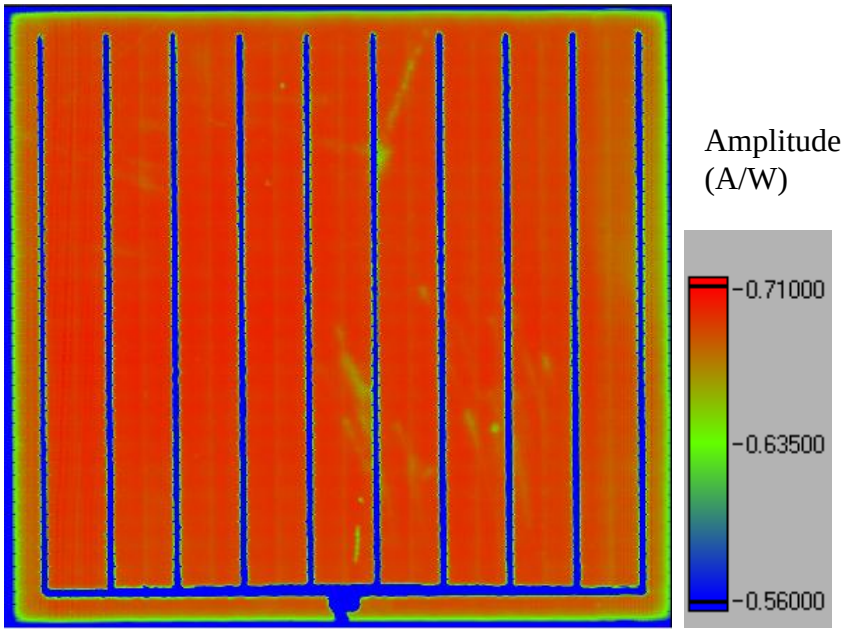

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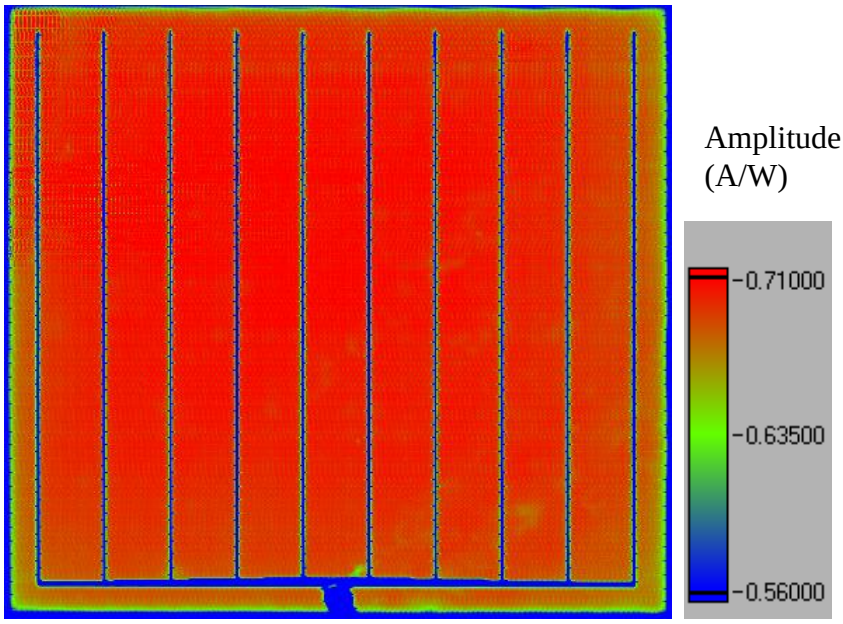

(d)

Figures 6.5: Long wavelength LBIC responses of solar cells with: (a)-(c) rear surfaces planarized with KOH using different recipes, (d) polished rear surface

6.3 Fabrication of LBSF Cells on 180 µm Thick mCz Substrates

While these results address the surface roughness, thickness and lifetimes differences also need to be studied. As an initial step, 4 cm^2 cells were fabricated on 180 µm thick magnetically stabilized Cz wafers (mCz). These wafers were chosen since they have a higher lifetime (>300 µs) compared to Cz which, based on the simulation results (figure 6.1), should lead to cell performance similar to FZ. Full Al BSF cells were also fabricated as a reference. Table 6.2 shows that results and trends are comparable to cell performance on thick FZ substrates. Cells on average had a slightly lower J_{sc} than the best FZ wafers, which is attributed to the thinner bulk material, but high cell V_{OC} of 655 mV and FF of 78.3% ensured a peak efficiency of 20.1%. This suggests that thinner substrates with rear surfaces planarized by KOH are capable of high efficiency with sufficiently high bulk lifetimes.

Table 6.2: Summary of cell results on 180 µm thick mCz substrates

Cell		V_{OC} (V)	J_{SC} (mA/cm^2)	Eff (%)	FF (%)
mCz Delta STAR	Avg	0.655	38.1	19.5	78.3
	Best	0.656	38.6	20.1	79.4
mCz Full BSF	Avg	0.640	36.7	18.5	78.7
	Best	0.642	37.1	18.9	79.4

6.4 LBSF Cell Fabrication on Thinner (160 µm) Cz Substrates

The next step was to fabricate local BSF cells on thinner (160 µm) commercial grade Cz wafers. The rear surfaces of these wafers were planarized similar to the mCz wafers discussed above and the same fabrication sequence was employed. The best 4 cm^2 Cz cell from this experiment is shown in Table 6.3. Peak efficiency reached was 19.3 %. Even though cell V_{OC} was similar to that predicted by PC1D (651 mV), the J_{SC} and FF were lower, leading to an efficiency that is significantly lower than the modeled values. While PC1D modeling allowed us to understand trends and predict performance, it fails to include actual material differences between FZ and Cz, which could influence the quality of passivation

Table 6.3: Cell parameters of the best LBSF cell on a Cz substrate

Cell		V_{OC} (V)	J_{SC} (mA/cm^2)	Eff (%)	FF (%)	n-factor	R_{Series}	R_{Shunt}
Cz Delta-STAR	Best Cell	0.651	38.4	19.3	77.3	1.34	0.54	10390

6.5 Understanding the Impact of Substrate Resistivity on LBSF Cells

PC1D simulations (Fig 6.6) were performed to compare the response of LBSF cells and full Al BSF cells to higher substrate resistivity. In the case of full Al BSF cells, cell V_{OC} and FF decrease even though the BSRV improves with higher resistivity, resulting in appreciable decrease in cell efficiency. In the case of LBSF cell structure, the loss in

efficiency is much more gradual, assuming the effective BSRV remains insensitive to resistivity. This is because, possible improvement in dielectric passivation on higher resistivity substrates is negated by more rear contact points or a higher metal area fraction to minimize the resistive losses. Thus resistivity of about 1 Ω.cm seems to be optimal for the local BSF cell.

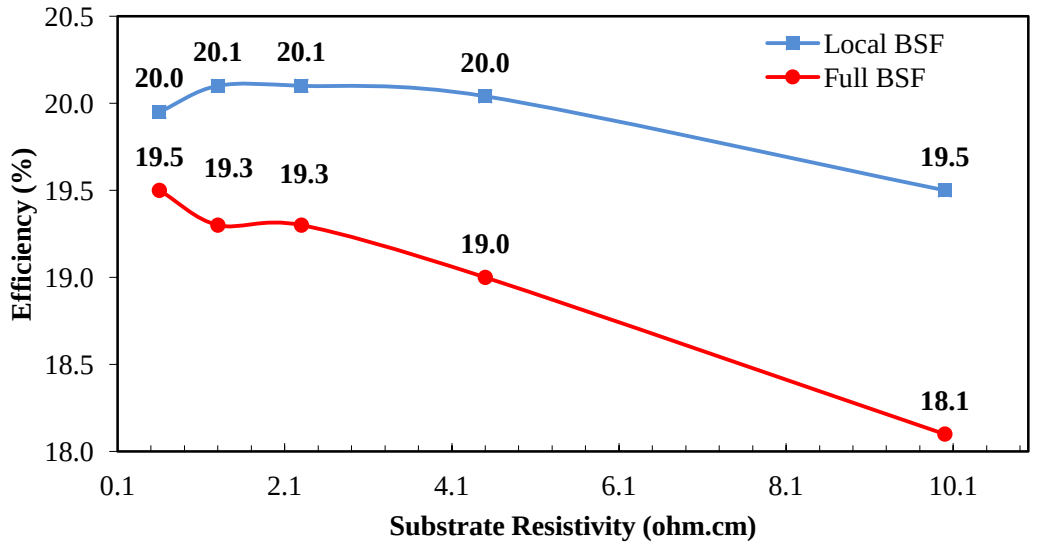

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Figure 6.6: Results of simulations comparing LBSF and full BSF cells on varying substrate resistivity

Experiments were performed to support this modeling. Rear dielectric was annealed and capped with PECVD SiN_x. Samples were prepared on wafers with resistivity ranging from 0.6 ohm.cm to 10 ohm.cm. Effective lifetimes were measured at various stages of processing and the surface recombination velocity was calculated at each stage using the formula

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2s}{W}$$

... (6.1)

where W is the wafer thickness. By assuming a sufficiently high bulk lifetime (~2 ms), the upper limit of the recombination velocity can be calculated.

These results are plotted as a function of the substrate doping density and can be seen in Figure 6.7. It was found that as the resistivity increases the surface recombination velocity of the dielectric stack decreases sharply.

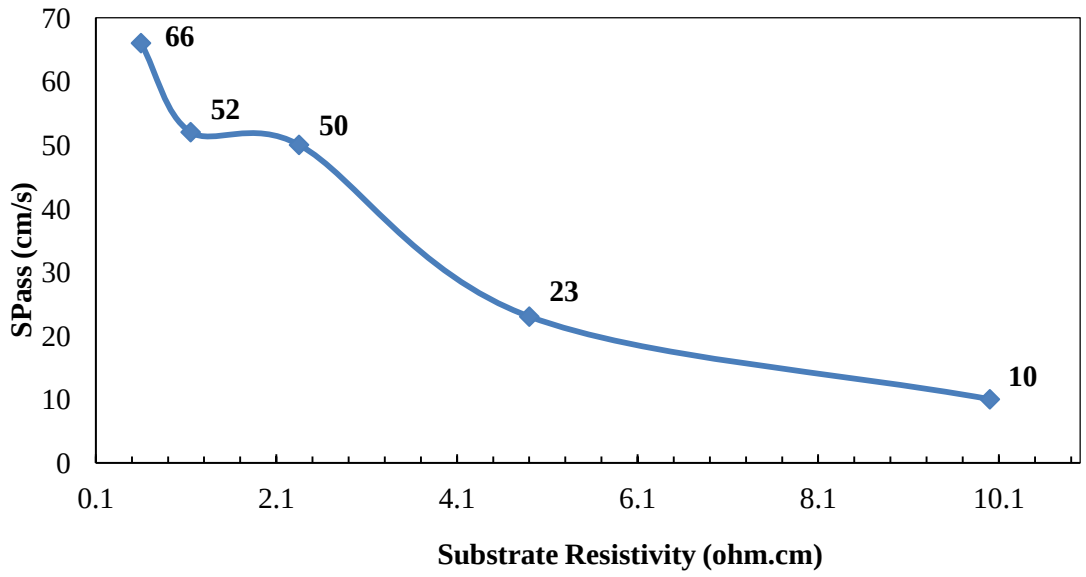

Figure 6.7: Dependence of surface recombination velocity on substrate resistivity

In order to ensure that the cells do not suffer a significant loss from series resistance at the rear contacts, the metal fraction is increased for higher resistivity substrates. A study on rear passivated structures provides a model for calculating the effective recombination velocity for similar cell structures [90].

$$S_{eff} = \frac{D_e}{W}\left(\frac{L_P}{2W\sqrt{\pi f}}arctan\left(\frac{2W}{L_P}\sqrt{\frac{\pi}{f}}\right) - exp\left(-\frac{W}{L_P}\right) + \frac{D_e}{fWS_{met}}\right)^{-1} + \frac{S_{pass}}{1-f}$$

…..(6.2)

where S_{eff} is the effective passivation of the metal-dielectric combination, S_{met} is the surface recombination at the metal contacts, S_{pass} is the recombination velocity at the dielectric-Si interface, D_e denotes the diffusion constant of the minority carriers, f is the metal area fraction ,L_p is the contact pitch and W is the thickness of the substrate. Another study on locally contacted cell structures provides calculated values for S_{met} for various substrate resistivities [91].

This analytical expression was used to fit the data acquired through modeling and characterization of the best LBSF cell and the results were in agreement with the earlier study. Hence using this formula, the aforementioned values of the S_{pass} and the calculated S_{met} values, S_{eff} was extracted for the various resistivities being studied in this work. The calculated values are shown in table 6.4. It is seen that while the calculated S_{eff} of 125 cm/s matches the modeled value for 2.35 ohm.cm substrates, other substrates have a lower S_{eff}. This indicates that assuming a BSRV of 125 cm/s as an extreme case for all substrates in subsequent simulations is realistic and viable.

Table 6.4: Summary of parameters used in extraction of Seff values for different substrate resistivity

Resistivity	Pitch	Spass	Smetal	Seff
0.6	0.12	66	200000	101.90
1.15	0.10	52	30000	105.14
2.35	0.08	50	20000	125.39
4.9	0.07	23	5000	93.84
10	0.05	10	2000	90.83

This study would require further simulation and experiments to fabricate, characterize and obtain the actual relation between the cell performance and substrate resistivity. Based on modeling and calculations, rear passivation in local BSF cells appears less sensitive to substrate resistivity.

6.5.1 Modeling and Understanding of the Impact of Light Induced Degradation on Delta-STAR Cells

Another important aspect of using Cz substrates is light induced degradation (LID). LID is now a well understood phenomenon in Boron doped Cz substrates attributed to formation of B-O complexes in the bulk material when exposed to sunlight, resulting in decreased bulk lifetime and cell performance [97]. LID is a significant factor in the overall performance and revenue from solar cells as it can result in an efficiency loss of 0.2-1% (absolute) in lower resistivity substrates (1-2 Ω.cm). Since this is directly related to the B doping level of the substrate, it is widely considered more beneficial to use higher resistivity subtrates or Ga-doped substrates to reduce or counter the effect of LID (Table 6.5 [98]).

Table 6.5: Summary of averaged results from different Cz substrates [98]

Dopant Type	Resistivity (ohm.cm)	Efficiency (%) – Annealed	Efficiency (%) – Stabilized
Boron	~1.0	16.7	15.6
	~4.3	17.0	16.4
Gallium	0.57-2.54	17.1	17.1

Preliminary simulations and calculations were performed to estimate the performance and LID in local BSF Cz cells. Using the best FZ cell as a template, a PC1D model was used to estimate the peak performance of Cz cells with different substrate doping. As with the earlier models, the BSRV of these cells was assumed constant and a nominal bulk lifetime was used for the simulations. A study on B-doped Cz substrates [99] provides a model to calculate the final bulk lifetime after LID as a function of substrate doping and Oxygen content in the Si.

$$\tau_{Cz} = 2 \times 7.675 \times 10^{45} [B_S]^{-0.824} [O_i]^{-1.748} \quad (6.3)$$

The final bulk lifetimes were calculated from this formula and used in the simulations to model the final cell efficiencies after LID. Figure 6.8 shows that the cell efficiencies decrease sharply at higher resistivity as the bulk series resistance lowers FF and the V_{OC} also drops. Even though the LID effect is smaller at higher resistivity, the absolute efficiency is lower. More experimental work needs to be done to validate these findings.

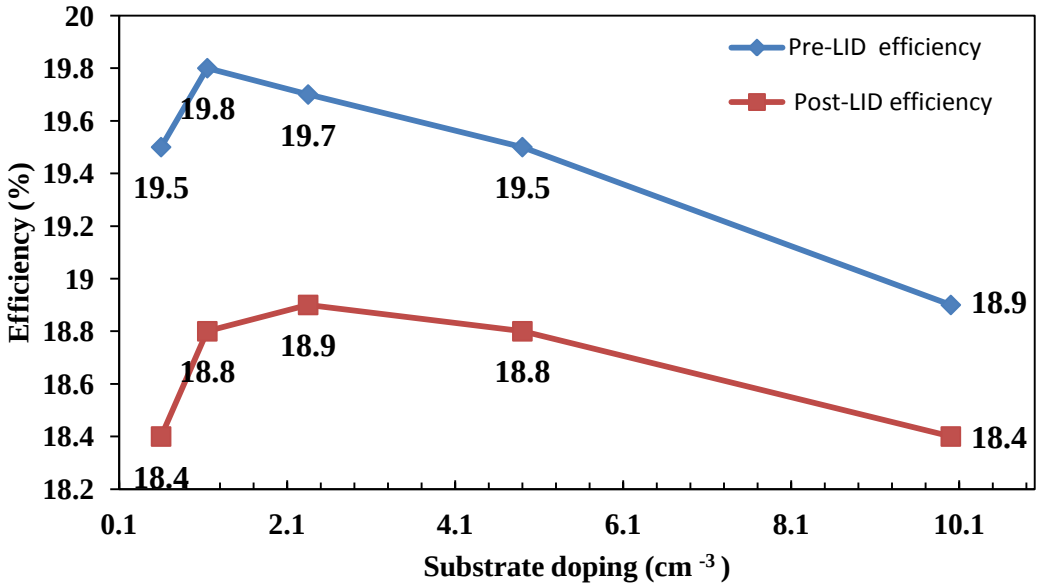

Figure 6.8: Modeled Cell efficiency before and after LID for local BSF cells on different substrate resistivities

6.6 Conclusion

In this chapter, the local BSF technology developed in earlier chapters was successfully applied on thin, commercial grade and lower bulk lifetime substrates. PC1D modeling was used to identify advantages of thinner, manufacturable substrates and establish efficiency targets. Transferring the technology from smoothly polished FZ surfaces to mCz and Cz required an investigation of the surface planarization processes. Optimization of rear surface planarization was achieved through surface roughness measurements, cell fabrication and LBIC analysis. As a result of this research, cell efficiency of ~20% was obtained on thin (180 µm) mCz substrates and 19.4% on thinner (160 µm) Cz wafers. PC1D modeling was used to study the effect of substrate resistivity

on LBSF cell efficiencies. Based on experimental data on surface passivation studies and device modeling, Cz substrate resistivities of 1-3 ohm.cm were found to be optimal for solar cell performance after LID.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

This thesis successfully demonstrated the use of spin-on solutions in the fabrication of high efficiency cells. A diffusion process was designed using in-house developed Phosphoric acid dopant solutions and optimized to produce emitters with high surface concentration and optimal emitter profile. The process was also modified and improved to make it insensitive to ambient humidity, which has been a challenge for most conventional spin-on sources. All these improvements led a high quality passivated emitter with a low emitter saturation current density of < 100 fA/cm^2. This emitter was first used to fabricate full Al BSF conventional cells (4 cm^2) with screen printed contacts, which led to cell efficiencies > 19.0%. This high quality emitter was then used with a spin-on dielectric for the fabrication of a local BSF cell structure that involves more than 95% of the rear surface passivated by a dielectric with local contacts over the remaining area. Fabrication of such a device would generally require multiple high temperature steps. A simple streamlined process was designed that produced a diffused and passivated device in just a single high temperature step during which phosphorous diffusion and in-situ oxidation was performed. Peak efficiencies of ~20% were obtained on research size 4 cm^2 cells. Nine 4 cm^2 cells were fabricated on 4 inch diameter FZ substrates. Characterization of these cells revealed that this improved efficiency for the local BSF cells resulted from an improvement in BSRV from 325 cm/s to 125 cm/s and in BSR from 67% to 93% compared to full BSF cells. These two factors contributed equally (~0.5) to the efficiency increase of 1% (absolute) for local BSF cells compared to their

counterpart baseline cells. Screen-printed etching process was used first to define the local vias through the dielectric but was found to be non-uniform, resulting in inconsistent solar cell performance. However, it did produce 20% efficient cells in the best case. Several laser candidates were investigated to solve this process reproducibility issue. Nanosecond UV laser was used to successfully replace the screen-printed etching method without reproducibility issues. Laser ablation was optimized to achieve 20% efficiency with two different rear contact geometries using single and five-pulse designs, thereby improving process flexibility and throughput.

To improve the manufacturability of these local BSF devices, they had to be fabricated on more inexpensive commercial substrates. Modeling was performed to identify the effect of substrate thickness and bulk lifetime on local BSF cell efficiency. Since the development work involved polished FZ wafers, first the effect of surface finish on these devices was investigated. Surface roughness was tailored using KOH solution based treatments. Local BSF cells fabricated on double side textured wafers failed and it was found that reduced surface roughness was very critical for rear passivation and cell performance. KOH planarized rear surface with an average surface roughness of ~0.75 μm was found to be adequate. Using such surfaces cell efficiencies of ~20% on 180 μm mCz and ~19.4% on 150 μm Cz substrates were achieved. PC1D modeling was used to study the effect of substrate resistivity on LBSF cell efficiencies. Based on experimental data on surface passivation structures and device modeling, it was concluded that Cz substrate resistivities of 1-3 ohm.cm were optimum for local BSF solar cell performance after LID.

This research has developed technology and prototype cells to provide guidelines for fabrication of high efficiency solar cells using a local BSF design. When implemented correctly, the local BSF design can improve cell efficiency significantly (~1% absolute) over the conventional full Al BSF devices on thinner and inexpensive substrates. This cell design can provide a reduction in the $/W of solar energy and bring PV technology closer to grid parity.

Transfer of technology to large wafers typically results in loss of efficiency due to higher series resistance, metal coverage and inhomogeneities resulting from larger substrates. In the following sections, several improvements for this technology are outlined that would assist in the transfer of this local BSF cell design to larger substrates while improving the performance and robustness of this technology.

7.1 Improvement of Front Contacts for Increased Efficiency of LBSF Cells

As mentioned above, an increase in substrate size results in increased metal coverage, from ~5% for 4 cm^2 to ~8% for large area cells, to compensate for the series resistance losses associated with the need for two bus-bars as well as carriers traversing longer distances in the front emitter. Increased metal coverage causes an increase in recombination at the metal-silicon interface and increases metal coverage or shading, which reduces J_{SC}. PC1D simulations show that this could lead to ~0.5-1.0 % (absolute) loss in efficiency. To compensate for these losses, a change in front contact metallization process is recommended. While screen printed contacts are inexpensive and quick,

studies have shown that only a small percentage of the entire line width participates in the collection of carriers from the underlying silicon [99]. Based on this, a reduction in the overall width of front contacts using alternate metallization techniques can achieve lower front metal coverage, while maintaining low contact resistivity. Other forms of contacts, such as plating combined with newer technologies such as inkjet printing have been shown to be viable candidates [100, 101]. These methods when combined with selective emitter technology can help achieve cell efficiencies of >19.5% on large substrates using this local BSF concept.

7.2 Improved Rear Contact Formation for Better LBSF Cells

The local BSF device studied in this thesis involved a very specifically designed rear contact metal. The Al paste used in this particular work lacked an aggressive glass frit and had 12% of silicon mixed into it. These two factors helped form a good local BSF while maintaining a high quality dielectric passivation in the surrounding regions. However, this resulted in lower adhesion of the fired Al contacts, which makes this Al unsuitable for use in large scale production. In addition, the lack of an aggressive glass frit in the Al paste also caused a very high sensitivity to index of the underlying SiN_X coating. The use of silicon rich SiN_X coatings were found to result in complete lack of adhesion for the Al paste. As a result, future work is required in developing an optimal real Al paste with high adhesion strength and low sensitivity to the index of the underlying dielectric, while preserving passivation of the surrounding dielectric.

An alternate method of rear contact formation could also be investigated in future. Ongoing studies have shown the use of lasers for local Boron doping [102]. Since this local BSF cell design already incorporates a laser ablation process, future research should focus on combining these processes to form a local BSF using spin-on Boron solutions. This method would isolate formation of the local BSF from the local contact formation process. Electro- and electroless plating could be used to selectively plate metal only in the Boron diffused local regions, which could be combined with the use of low-curing rear pastes such as Ag/Al that would provide increased conductivity and rear reflectance. This processing route would reduce the dependence on modified Al pastes which suffer from the adhesion problems.

7.3 Improved Rear Passivation for Increased LBSF Cell Efficiency

In this research, 20% cells were achieved by improving BSRV and BSR compared to standard full BSF cells. Replacing the existing rear contact paste with alternate metallization schemes could lead to a BSR higher than the 93% achieved in this study. BSR values of 98% are possible. A BSRV of 125 cm/s was achieved in the high efficiency cells described in this research. To improve cell efficiencies beyond 20%, alternate dielectrics need to be considered to replace the oxide/SiN_x dielectric stack developed in this research. Recent studies have shown that negatively charged Al_2O_3 is capable of providing very high quality surface passivation on p-Si, resulting in cell efficiencies of ~21% with a BSRV <80 cm/s [103]. Recently, high throughput methods of depositing Al_2O_3 have been reported [104, 105], making it attractive for future local BSF devices with efficiencies approaching 21%.

REFERENCES

1. National Oceanic and Atmospheric Administration Report, 2010.
2. U.S. Energy Information Administration (EIA), "*Annual Energy Review*," 2010.
3. U.S. Energy Information Administration (EIA), Form EIA-63B, *"Annual Photovoltaic Module/Cell Manufacturers Survey"*.
4. US Department of Energy, *"Solar energy technologies program: Multi-year program plan 2007-2011 and beyond,"* Washington, DC, 2006.
5. A. Rohatgi, A. Ristow, A. Das and S. Ramanathan, *"Road to Cost effective Si PV", Proc. 18th International PVSEC,* Kolkata, 2009.
6. O.Babinet, D.Gellman,J.Trkulja, *"Solar's push to reach mainstream",* Deloitte Review, No.5, 2009.
7. J. Zhao, A. Wang, P. Campbell, and M. A. Green, *"A 19.8% efficient honeycomb multicrystalline silicon solar cell with improved light trapping",* Electron Devices, IEEE Transactions on, vol. 46, pp. 1978-1983, 1999.
8. K. Fukui, S. Goto, J. Atobe, H. Hashigami, Y. Sakai, M. Tsuchida, Y. Inomata, S. Fujii, and K. Shirasawa, *"17.7% efficiency large area multicrystalline silicon solar cell using screen-printed metallization technique",* 2005, pp. 979-982.
9. D.A. Clugston and P.A. Basore, *"PC1D Version 5: 32-bit solar cell modeling on personal computers",* Proc. 26th IEEE Photovoltiac Specialists Conference, Anaheim, pp. 207–210, 1997.
10. W. Shockley and W. T. Read, *"Statistics of the recombinations of holes and electrons,"* Physical Review, vol. 87, pp. 835-842, 1952.

11. R. N. Hall, *"Electron-hole recombination in germanium,"* Physical Review, vol. 87, pp. 387, 1952.
12. A. G. Aberle, "*Advanced surface passivation and analysis*", Centre for Photovoltaic Engineering, University of New South Wales, 1999.
13. S. W. Glunz, A. Grohe, M. Hermle, M. Hofmann, S. Janz, T. Roth, O. Schultz, M. Vetter, I. Martin, R. Ferre, S. Bermejo, W. Wolke, W. Warta, R. Preu, and G. Willeke, "*Comparison of different dielectric passivation layers for application in industrially feasible high-efficiency crystalline silicon solar cells,"* Proceedings of the 20th EU-PVSEC, 2005, pp. 572-577.
14. B.L. Sopori and T. Marshall, Proc. IEEE PVSC (Piscataway,NJ: IEEE, 1993), p. 127.
15. M. A. Green, A. W. Blakers, J. Zhao, A. M. Milne,A. Wang, and X. Dai, "*Characterization of 23-Percent Efficient Silicon Solar Cells",* IEEE Transactions on Electron Devices. 37(2), February 1990.
16. M. A. Green, "*Recent progress in crystalline and polycrystalline silicon solar cells",* Solar Energy Materials 23 (1991) 111-116.
17. R. Hezel and K. Jaeger, *"Low-Temperature Surface Passivation of Silicon for Solar Cells,"* Journal of the Electrochemical Society, vol. 136, p. 518, 1989.
18. A. G. Aberle and R. Hezel, *"Progress in Low-temperature Surface Passivation of Silicon Solar Cells using Remote-plasma Silicon Nitride," Progress in Photovoltaics: Research and Applications,* vol. 5, pp. 29-50, 1997.
19. A.G.Aberle, T. Lauinger, R. Hezel, *"Remote PECVD silicon nitride—a key technology for the crystalline silicon PV industry of the 21st century",* Proceedings of

the 14th European Photovoltaic Specialists Conference, Barcelona, 1997,pp. 684–689.

20. S.W. Glunz,R. Preu,S. Schaefer,E. Schneiderlöchner, W. Pfleging, R. Lüdemann, G. Willeke, *"New simplified methods for patterning the rear contact of RP-PERC high-efficiency solar cells*", Proceedings of the 28th IEEE Photovoltaic Specialists Conference, Anchorage, 2000; 168–171.
21. S. Dauwe, A. Metz, R. Hezel, *"A novel mask-free low-temperature rear surface passivation scheme based on PECVD silicon nitride for high-efficiency silicon solar cells",* Proceedings of the 16th European Photovoltaic Specialists,Conference, Glasgow, 2000; 1747–1750.
22. S. Dauwe, L. Mittelstadt, A. Metz, J. Schmidt, and R. Hezel, "*Low-Temperature Rear Surface Passivation Schemes For > 20 % Efficient Silicon Solar Cells",* Proceedings of the 3rd World Conference on Photovoltaic Energy Conversion May 11-18,2003.
23. J. Schmidt, M. Kerr, and A. Cuevas, *"Surface passivation of silicon solar cells using plasma-enhanced chemical-vapour-deposited SiN films and thin thermal SiO_2/plasma SiN stacks,"* Semiconductors Science and Technology, vol. 16, pp. 164-170, 2001.
24. D. L. King, B. R. Hansen, J. A. Kratochvil, and M. A. Quintana, *"Dark current-voltage measurements on photovoltaic modules as a diagnostic or manufacturing tool,"* 1997, pp. 1125-1128.
25. K.R. McIntosh, C.B. Honsberg, *"A new technique for characterizing floating-junction-passivated solar cells from their dark IV curves",* Progress in Photovoltaics: Research and Applications 1999; 7(5): 363–378.

26. K.R.Macintosh, *"Lumps,humps and bumps: Three Detrimental effects in C-V curves of solar cells",* Doctoral Thesis, University of New South Wales, 2001.

27. S. Dauwe, J. Schmidt, and R. Hezel, *"Very low surface recombination velocities on p- and n-type silicon wafers passivated with hydrogenated amorphous silicon films"*, Proceedings of the 29th IEEE PVSC, 2002, pp. 1246-1249.

28. P.P.Altermatt, G. Heiser, X. Dai,J. Jürgens, A.G. Aberle, S.J. Robinson, T. Young, S.R. Wenham, M.A. Green , *"Rear surface passivation of high-efficiency silicon solar cells by a floating junction",* Journal of Applied Physics 1996; 80: 3574–3586.

29. C. B. Honsberg, S. B. Ghozati, A. Ebong, Y. H. Tang, and S. R. Wenham, *"Elimination of parasitic effects in floating junction rear surface passivation for solar cells,"* in 25th IEEE PVSC, 1996, pp. 401-404.

30. A. G. Aberle, S.W. Glunz, and W. Warta, *"Impact of illumination level and oxide parameters on Shockley-Read-Hall recombination at the Si-SiO2 interface"*, Journal of applied physics, vol. 71, pp. 4422-4431, 1992.

31. J. Y. Lee and S.W. Glunz, "*Investigation of various surface passivation schemes for silicon solar cells",* Solar Energy Materials & Solar Cells 90 (2006) 82–92.

32. O. Schultz, A. Mette, M. Hermle and S.W. Glunz, "*Thermal Oxidation for Crystalline Silicon Solar Cells Exceeding 19% Efficiency Applying Industrially Feasible Process Technology",* Prog. Photovolt: Res. Appl. 2008; 16:317–324.

33. B.E.Deal, "*Thermal oxidation kinetics of silicon in pyrogenic H_2O and 5% HCl/H_2O mixtures",* Journal of the Electrochemical Society 1978; 125:576–579.

34. P.B.Moynagh and P.J.Rosser, "*In Properties of Silicon"*,The Institution of Electrical Engineers: London and New York, 1987; 469–479.

35. M.Hörteis, D.Grote, S.Binder, A.Filipovic, D.Schmidt and S.W. Glunz, "*Fine line printed and plated contacts on high ohmic emitters enabling 20% cell efficiency",* Conference Record of the IEEE Photovoltaic Specialists Conference, p 60-65, 2009.
36. L. Gautero, M. Hofmann, J. Rentsch, A. Lemke, S. Mack, J. Seiffe, J. Nekarda,D. Biro, A. Wolf, B.Bitnar, J. Sallese and, R. Preu, "*All-screen-printed 120-µm-thin large-area Silicon Solar Cells Applying dielectric Rear Passivation and Laser-fired Contacts Reaching 18% efficiency",* Proceedings of the 33rd IEEE PVSC, June 2009, Philadelphia.
37. S. Gatz, H. Hannebauer, R. Hesse, F. Werner, A. Schmidt, T. Dullweber, J. Schmidt, K. Bothe, and R. Brendel, *"19.4% efficient large area fully screen printed silicon solar cells,"* Physica Status Solidi (RRL) Rapid Research Letters, vol. 5, pp. 147–149, 2011.
38. J. Lai, A. Upadhyaya, S. Ramanathan, A. Das, K. Tate, V. Upadhyaya, A. Kapoor, C. Chen, and A. Rohatgi, *"High-Efficiency Large-Area Rear Passivated Silicon Solar Cells With Local Al-BSF and Screen-Printed Contacts,"* IEEE Journal of Photovoltaics, vol.1, pp. 16-21, 2011.
39. K. A. Münzer, J. Schöne, A. Teppe, M. Hein, R. E. Schlosser, M. Hanke, K. Varner, H. Mäckel, S. Keller, and P. Fath, "*Physical properties of industrial 19% rear side passivated Al-LBSFR-solar cells,"* Energy Procedia, vol. 8, pp. 415-420.
40. G. Agostinelli, A. Delabie, P. Vitanov,Z. Alexieva,H.F.W. Dekkers,S. De Wolf,G. Beaucarne, *"Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge",* Solar Energy Materials and Solar Cells 2006; 90: 3438– 3443.

41. B. Hoex, S.B.S. Heil, E. Langereis, M.C.M. van de Sanden and W.M.M. Kessels. "*Ultralow surface recombination of c-Si substrates passivated by plasma-assisted atomic layer deposited Al_2O_3",* Applied Physics Letters 2006; 89: 042112/1-3.

42. J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M. C. M. van de Sanden and W. M. M. Kessels, "*Surface Passivation of High-efficiency Silicon Solar Cells by Atomic-layer-deposited Al_2O_3",* Prog. Photovolt: Res. Appl. 2008; 16:461–466.

43. M. Hofmann, S. Glunz, R. Preu and G. Willeke, *"21%-Efficient Silicon Solar Cells using Amorphous Silicon Rear Side Passivation",* 21st Eu-PVSEC, September 2006, Dresden.

44. Y.Tsunomura, Y.Yoshimine, M.Taguchi, T. Baba, T.Kinoshita, H.Kanno, H.Sakata, E.Maruyama and M.Tanaka, *"Twenty-two percent efficiency HIT solar cell",* Solar Energy Materials and Solar Cells, v 93, n 6-7, p 670-673, June 2009.

45. R. Low, A. Gupta, N. Bateman, D. Ramappa, P. Sullivan, W. Skinner and J. Mullin, "*High efficiency selective emitter enabled through Patterned ion implantation",* 35th IEEE PVSC, Hawaii,2010.

46. S. Queisser, E. Wefringhaus, M. Lichtner, W. Saule, A. Heeren, F. Delahaye and J. Schweckendiek, "*Novel Precursor Deposition Method For Inline Diffusion",* Eu-PVSEC, Valencia 2008.

47. C.Voyer, D.Biro, G.Emanuel,R. Preu,J. Kariath and H.Wanka, 2004, 19th European Photovoltaic Solar Energy Conf. (Paris, France, 7–11 June 2004).

48. J. Monkowski and J. Stach, Solid State Technol., 19, 38, ~1976.

49. B.Herzog and K.Peter 2006 22nd European Photovoltaic Solar Energy Conf. (Dresden, Germany, 4–8 September 2006).

50. C.Voyer, N.G. Tarr, R.E. Thomas, and S. Varma, "*Infrared emitter diffusion using thin and heavily-doped phosphorus source layers"*, Proceedings of the 3rd World Conference on Photovoltaic Energy Conversion, v B, p 1415-1418, 2003.
51. C.Voyer, T.Buettner, R.Bock, D.Biro and R.Preu, "*Microscopic homogeneity of emitters formed on textured silicon using in-line diffusion and phosphoric acid as the dopant source"*, in 17th International Photovoltaic Science and Engineering Conference Fukuoka, Japan, 2007.
52. T. Krygowski, Doctoral Thesis, Georgia Institute of Technology, 1998.
53. D.Bouhafs, A.Moussi, M.Boumaour, S.E.K.Abadia, L.Mahiou, A.Messaoud, "*Influence of the organic solvents on the properties of the phosphoric acid dopant emulsion deposited on multicrystalline silicon wafers",* Journal of Physics D: Applied Physics, vol. 40, pp. 2728-2731, 2007.
54. T. Krygowski, A. Rohatgi, and D.S Ruby, "*Simultaneous P and B diffusion, in-situ surface passivation, impurity filtering and gettering for high-efficiency silicon solar cells",* Conference Record of the IEEE Photovoltaic Specialists Conference, p 19-24, 1997.
55. D.S. Kim, M.M. Hilali, A. Rohatgi, K. Nakano, A. Hariharan, and K. Matthei, "*Development of a phosphorus spray diffusion system for low-cost silicon solar cells",*Journal of the Electrochemical Society, v 153, n 7, p A1391-A1396, July 2006.
56. V. Meemongkolkiat, K.Nakayashiki, D.S. Kim, S. Kim, A. Shaikh, A. Kuebelbeck, W. Stockum and A. Rohatgi, "*Investigation of modified screen-printing AL pastes for local back surface field formation",* Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, WCPEC-4, v 2, p 1338-1341, 2007.

57. R.H.Micheels, and P.E. Valdivia , IEEE Trans Elec.Dev, 37, No 2 , p 353-354.

58. M.D. Abbott,J.E. Cotter, and K. Fisher, Proc. IEEE 4th WCPEC, v 1, p 988-991.

59. E. Schneiderlöchner, A. Grohe, C.Ballif, et al, Proc. IEEE PVSC, p 300-303, 2002.

60. P. Engelhart, N.P. Harder,T. Horstmann, R. Grischke,R. Meyer and R. Brendel, Proc. 4th WCPEC, Hawaii, p 1027-1027, 2006.

61. N. Mingirulli, A. Grohe, A. Dohrn, M. Hofmann, M. Schubert, T. Roth, D. Biro, and R. Preu, *"Lifetime studies on laser drilled vias for application in emitter-wrap-through solar cells,"* Proceedings of the 22nd European Photovoltaic Solar Energy Conference, Milan, Italy, 2007.

62. F. Clement, M. Menkoe, T. Kubera, C. Harmel, R. Hoenig, W. Wolke, H. Wirth, D. Biro, and R. Preu, *"Industrially feasible multi-crystalline metal wrap through (MWT) silicon solar cells exceeding 16% efficiency,"* Solar energy materials and solar cells, vol. 93, pp. 1051-1055, 2009.

63. Z. Hameiri, L. Mai, T. Puzzer, and S. R. Wenham, *"Influence of laser power on the properties of laser doped solar cells,"* Solar Energy Materials and Solar Cells.

64. C. Morilla, R. Russell, J. M. Fernandez, and B. P. S. Espana, *"Laser induced ablation and doping processes on high efficiency silicon solar cells," 23rd EUPVSEC,* 2008.

65. D. Kray, A. Fell, S. Hopman, K. Mayer, G. Willeke, S. Glunz, *"Laser Chemical Processing (LCP) A versatile tool for microstructuring applications",* Applied Physics A: Materials Science and Processing 93 (2008) 99–103.

66. A. Grohe, R. Preu, S. W. Glunz, and G. Willeke, *"Laser applications in crystalline silicon solar cell production,"* 2006, p. 619717.

67. A. Grohe, A. Harmel, C. Knorz, et al*,"Selective laser ablation of anti-reflection coatings for novel metallization techniques",* Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, v 2, p 1399-1402.

68. K. Mangersnes, S. E. Foss, and A. Thøgersen, *"Damage free laser ablation of SiO2 for local contact opening on silicon solar cells using an a-Si: H buffer layer,"* Journal of Applied Physics, vol. 107, pp. 043518-043518-6.

69. S. W. Glunz, M. Aleman, J. Bartsch, N. Bay, K. Bayer, R. Bergander, A. Filipovic, S. Greil, A. Grohe, and M. Horteis, *"Progress in advanced metallization technology at Fraunhofer ISE,"* 2008, pp. 1-4.

70. P. Engelhart, S. Hermann, T. Neubert, H. Plagwitz, R. Grischke, R. Meyer, U. Klug, A. Schoonderbeek, U. Stute, and R. Brendel, *"Laser ablation of SiO2 for locally contacted Si solar cells with ultra-short pulses,"* Progress in Photovoltaics: Research and Applications, vol. 15, pp. 521-527, 2007.

71. S. W. Glunz, R. Preu, S. Schaefer, E. Schneiderlochner, W. Pfleging, R. Ludemann, and G. Willeke, *"New simplified methods for patterning the rear contact of RP-PERC high-efficiency solar cells,"* 2000, pp. 168-171.

72. A. Grohe, C. Harmel, A. Knorz, S. W. Glunz, R. Preu, and G. P. Willeke, *"Selective laser ablation of anti-reflection coatings for novel metallization techniques,"* 2006, pp. 1399-1402.

73. S.Ramanathan, V.Meemongkolkiat,A.Das A.Rohatgi, I.Kohler, *"Fabrication of 20 % efficient cells using spin-on based simultaneous diffusion and dielectric anneal,"* in IEEE 34rd Photovoltaics Specialists Conference Philadelphia, 2009.

74. L. Mai, S. Wenham, B. Tjahjono, J. Ji, Z. Shi, *"New emitter design and metal contact for screen-printed solar cell front surfaces",* 4th IEEE World Conf. on Photovoltaic Energy Conversion, Hawaii, USA, 2006.

75. M. M. Hilali, B. To, and A. Rohatgi, *"A review and understanding of screen-printed contacts and selective emitter formation",* presented at Proceedings of the 14thWorkshop on Crystalline Silicon Solar Cells and Modules NREL, Winter Park, Colorado, USA, 2004.

76. J.J. Biernacki, R. Subramanian, M.R. Islam, C. Schewe, M.C. Rogers, *"Gas-phase mixing and dispersion in a diffusion furnace,"* Journal of the electrochemical society vol. 151, pp. 24-32, 2004.

77. D. Kane, R. Swanson, in IEEE photovoltaic specialists conference 18, (IEEE, New York, 1985, 1985), vol. 69, p. 578–583.

78. A. Ebong, M. Hilali, V. Upadhyaya, B. Rounsavilfe, I. Ebong, and A. Rohatgi, "*High Efficiency Screen-Printed Planar Solar Cells On Single Crystalline Silicon Materials"*, Conference Record of the IEEE Photovoltaic Specialists Conference, p 1173-1176, 2005.

79. T. Krygowski, Doctoral Thesis, Georgia Institute of Technology, 1998.

80. M.M. Hilali, K. Nakayashiki, A. Ebong, A. Rohatgi, "*High-efficiency (19%) screen-printed textured cells on low-resistivity float-zone silicon with high sheet-resistance emitters",* Progress in Photovoltaics: Research and Applications, v 14, n 2, p 135-144, March 2006.

81. G.K. Reeves and H.B. Harrison, *"Obtaining the specific contact resistance from transmission line model measurements"*, IEEE Electron Device Lett., 3 (1982) 11113.

82. V. Meemongkolkiat, Ph.D Thesis, Georgia Institute of Technology, 2008.

83. B. S. Richards, "*Comparison of TiO2 and Other Dielectric Coatings for Buried contact Solar Cells: A Review",* Prog. Photovolt: Res. Appl. 2004; 12:253–281.

84. B. Sopori, *"Dielectric films for Si solar cell applications,"* Journal of electronic materials, vol. 34, pp. 564-570, 2005.

85. S. Dauwe, L. Mittelstadt, A. Metz, R. Hezel, "*Experimental Evidence of Parasitic Shunting in Silicon Nitride Rear Surface Passivated Solar Cells,"* Progress in Photovoltaics: Research and Applications, vol. 10, pp. 271–278, 2002.

86. V. Meemongkolkiat, D. S. Kim, and A. Rohatgi, *"SiO2-based spin-on dielectrics for back surface passivation of p-type Si solar cells,"* 2007, pp. 3-7.

87. V. Meemongkolkiat, K. Nakayashiki, D.S. Kim, S. Kim, A. Shaikh, A. Kuebelbeck, W. Stockum and A.Rohatgi, *"Investigation of modified screen-printing AL pastes for local back surface field formation"*, Conference Record of the 2006 IEEE 4th World Conference on Photovoltaic Energy Conversion, WCPEC-4, v 2, p 1338-1341, 2007.

88. D.S. Kim, M.M. Hilali, A. Rohatgi, K. Nakano,A. Hariharan, and K. Matthei, "*Development of a phosphorus spray diffusion system for low-cost silicon solar cells",*Journal of the Electrochemical Society, v 153, n 7, p A1391-A1396, July 2006.

89. B. Fischer*,"Loss analysis of crystalline silicon solar cells using photoconductance and quantum efficiency measurements,"* Ph.D. thesis, University of Konstanz, 2003.

90. O. Schultz, A. Mette, M. Hermle and S.W. Glunz, "*Thermal Oxidation for Crystalline Silicon Solar Cells Exceeding 19% Efficiency Applying Industrially Feasible Process Technology",* Prog. Photovolt: Res. Appl. 2008; 16:317–324.

91. M.J. Loboda, G.A. Toskey, *"Understanding hydrogen silsesquioxane-based dielectric film processing",* Solid state technology, 1998, Vol 41, No. 5, pp. 99-105.

92. Semitest Surface Charge Analyzer 2500 - User Manual.

93. S. Dauwe, L. Mittelstadt, A. Metz, R. Hezel, *"Experimental Evidence of Parasitic Shunting in Silicon Nitride Rear Surface Passivated Solar Cells,"* Progress in Photovoltaics: Research and Applications, vol. 10, pp. 271–278, 2002.

94. T. Lauermann, T. Lüder, S. Scholz, B. Raabe, G. Hahn, and B. Terheiden, *"Enabling dielectric rear side passivation for industrial mass production by developing lean printing-based solar cell processes,"* Proceedings of the 35th IEEE PVSC, 2010, pp. 28-33.

95. S. Martinuzzi, M. Stemmer, *"Mapping of defects and their recombination strenght by a light-beam-induced current in silicon wafers",* Materials Science and Engineering: B, Volume 24, Issues 1–3, May 1994, Pages 152-158

96. S.W.Glunz,S. Rein, W. Warta, J. Knobloch, and W. Wettling, "*Degradation of carrier lifetime in Cz silicon solar cells",* Solar Energy Materials and Solar Cells, v 65, n 1, p 219-229, January 2001.

97. V. Meemongkolkiat, K. Nakayashiki, A. Rohatgi, G. Crabtree, J. Nickerson and T.L. Jester, "*The effect of the variation in resistivity and lifetime on the solar cells performance along the commercially grown Ga- and B-doped Czochralski ingots"*, Conference Record of the IEEE Photovoltaic Specialists Conference, p 1115-1118, 2005.

98. K.Bothe, R. Sinton and J.Schmidt, "*Fundamental Boron-Oxygen-related carrier lifetime limit in mono- and multicrystalline silicon",* Progress in Photovoltaics: Research and Applications 13,2005, pp 287-296.

99. M.M.Hilali, Doctoral Thesis, Georgia Institute of Technology, 2004.

100. E. Lee, H. Lee, J. Choi, D. Oh, J. Shim, K. Cho, J. Kim, S. Lee, B. Hallam, and S. R. Wenham, *"Improved LDSE processing for the avoidance of overplating yielding 19.2% efficiency on commercial grade crystalline Si solar cell," Solar Energy Materials and Solar Cells*.

101. A. Ebong, I.B. Cooper, B. Rounsaville, A. Rohatgi, M. Dovrat, E. Kritchman, D. Brusilovsky, A. Benichou, *"Successful Implementation of Narrow AG Gridlines with Ink Jet Machine for High Quality Contacts to Silicon Solar Cells",* Proceedings of the 26th European Photovoltaic Solar Energy Conference, pp.1711 – 1714, 2011.

102. N. Palina, T. Mueller, S. Mohanti, and A. G. Aberle, *"Laser Assisted Boron Doping Of Silicon Wafer Solar Cells Using Nanosecond And Picosecond Laser Pulses",* Proceedings of the 37th IEEE PVSC, 2011.

103. B. Hoex, M. C. M. van de Sanden, J. Schmidt, R. Brendel, and W. M. M. Kessels, "Surface passivation of phosphorus-diffused n+-type emitters by plasma-assisted atomic-layer deposited Al_2O_3", Phys. Status Solidi, RRL 6, No. 1, 4–6 (2012).

104. F. Werner, B. Veith, V. Tiba, P. Poodt, F. Roozeboom, R. Brendel, and J. Schmidt, *"Very low surface recombination velocities on p-and n-type c-Si by ultrafast spatial atomic layer deposition of aluminum oxide," Applied Physics Letters,* vol. 97, p. 162103.

105. S. Miyamjima, J. Irikawa, A. Yamada, and M. Konagai, *"Hydrogenated aluminum oxide films deposited by plasma enhanced chemical vapor deposition for passivation of ptype crystalline silicon", presented at Proceedings of the 23rd European Photovoltaic Solar Energy Conference*, 2008.

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